# CACHE OPTIMIZATION

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## Overview

- Announcement
  - Homework 4 will be released on Oct. 30th
- This lecture
  - Cache replacement policies
  - Cache write policies
- Reducing miss penalty

## Cache Replacement Policies

- Which block to replace on a miss?
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**Cache Set**

| | |
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**Requested Blocks**

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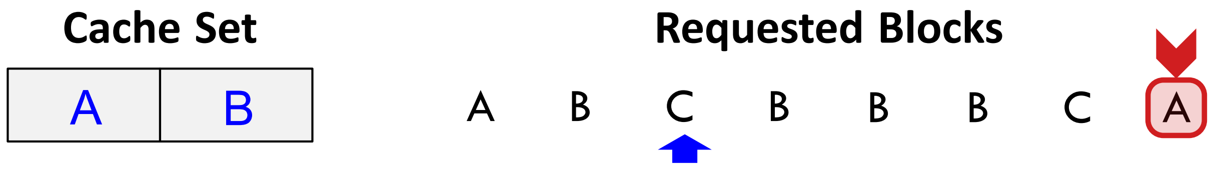

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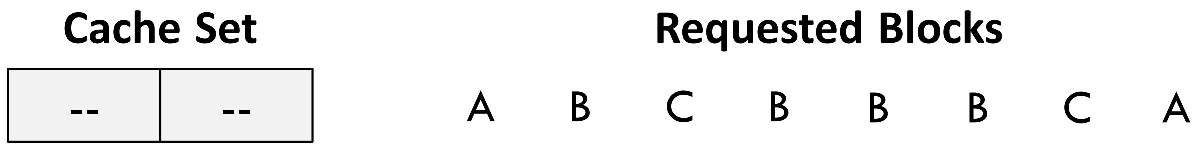

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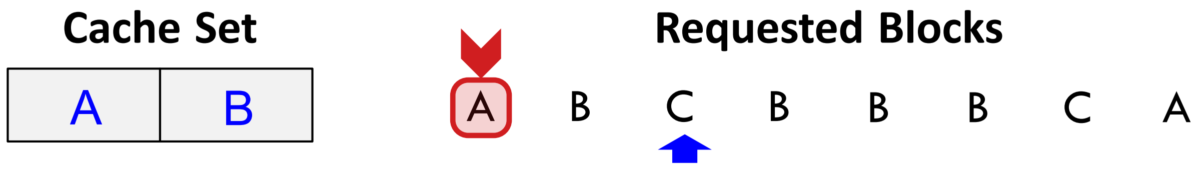

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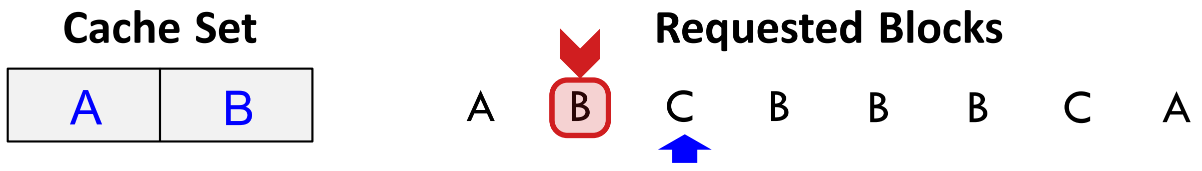

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- Least recently used (LRU)
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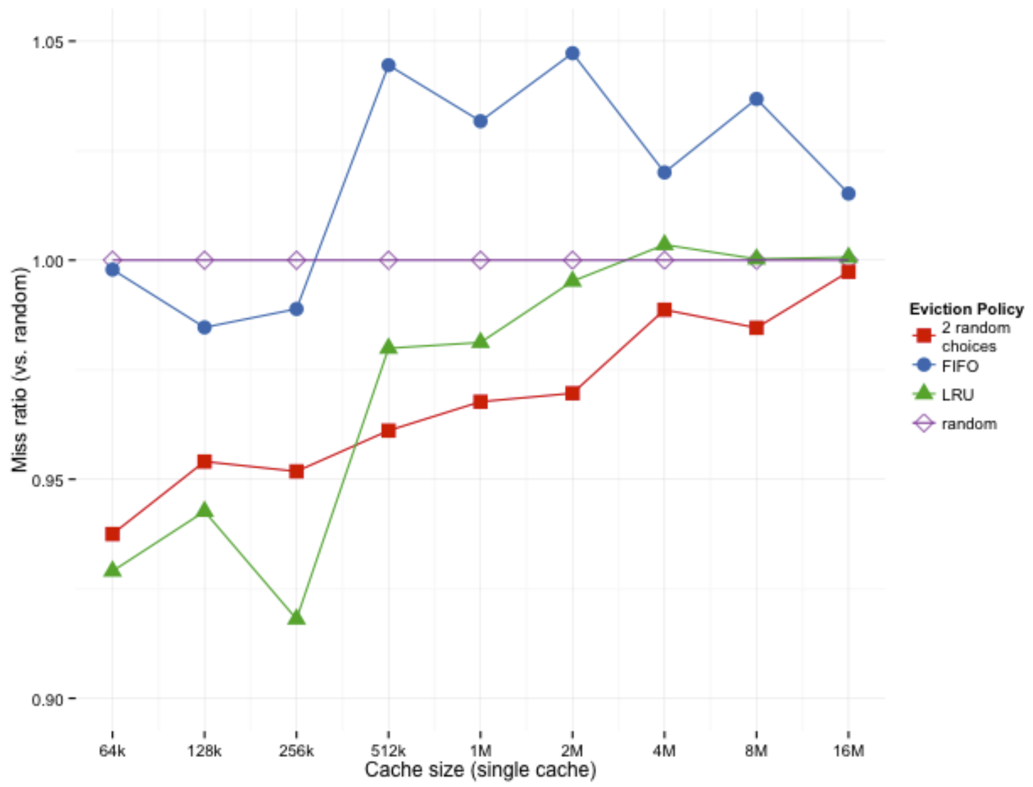
- Most recently used (MRU)
  - Replace the block accessed nearest in the past
- Random replacement
  - hardware randomly selects a cache block to replace

# Random vs. LRU

- 2-Random: choose two cache elements at random, and evict the least-recently-used one.

*Source: https://danluu.com/2choices-eviction/*



## Example Problem

- Blocks A, B, and C are mapped to a single set with only two block storages; find the miss rates for LRU and MRU policies.
- 1. A, B, C, A, B, C, A, B, C
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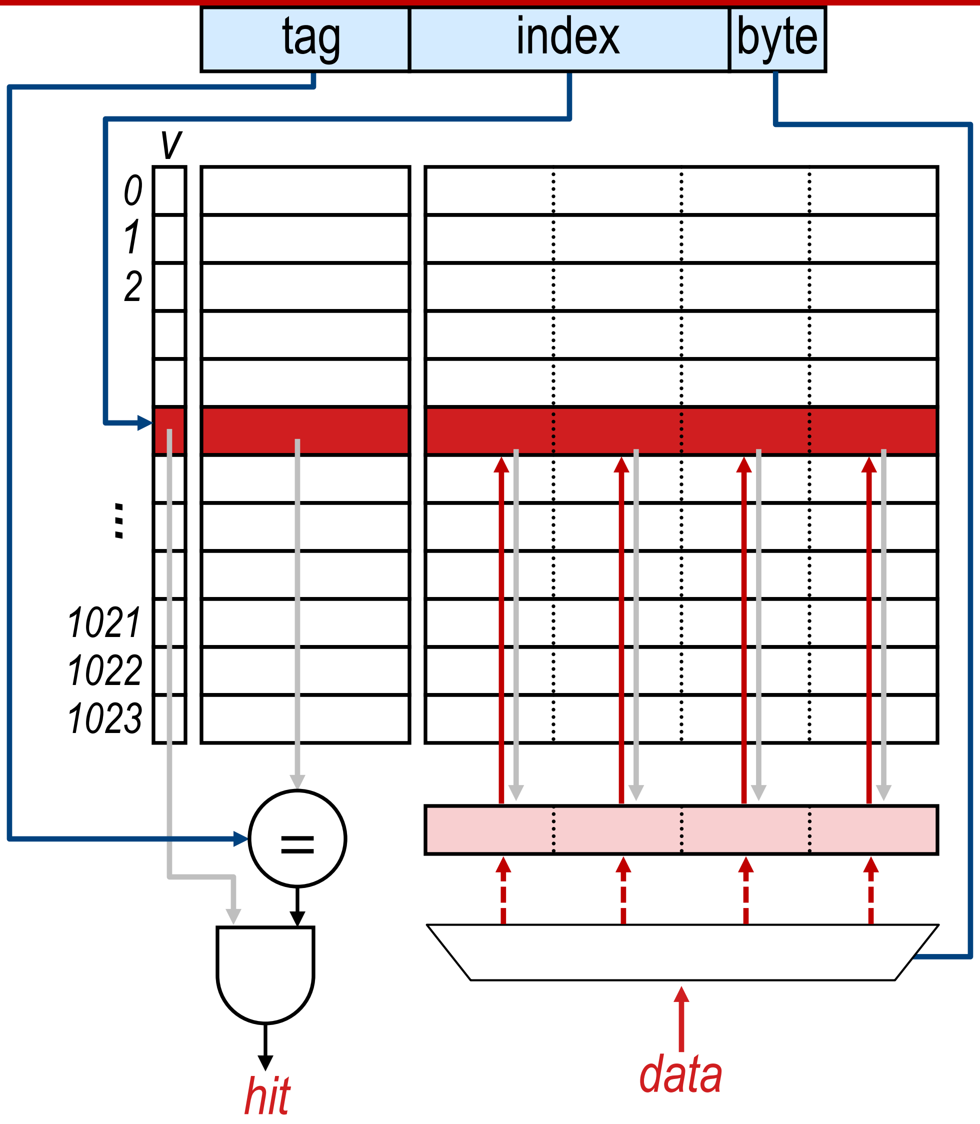
- 1. A, B, C, A, B, C, A, B, C
  - LRU : 100%
  - MRU : 66%
- 2. A, A, B, B, C, C, A, B, C
  - LRU : 66%
  - MRU : 44%

# Cache Write Policies

- Write vs. read



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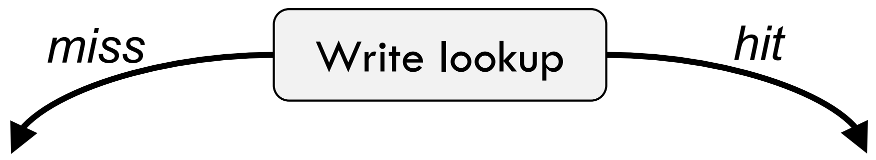

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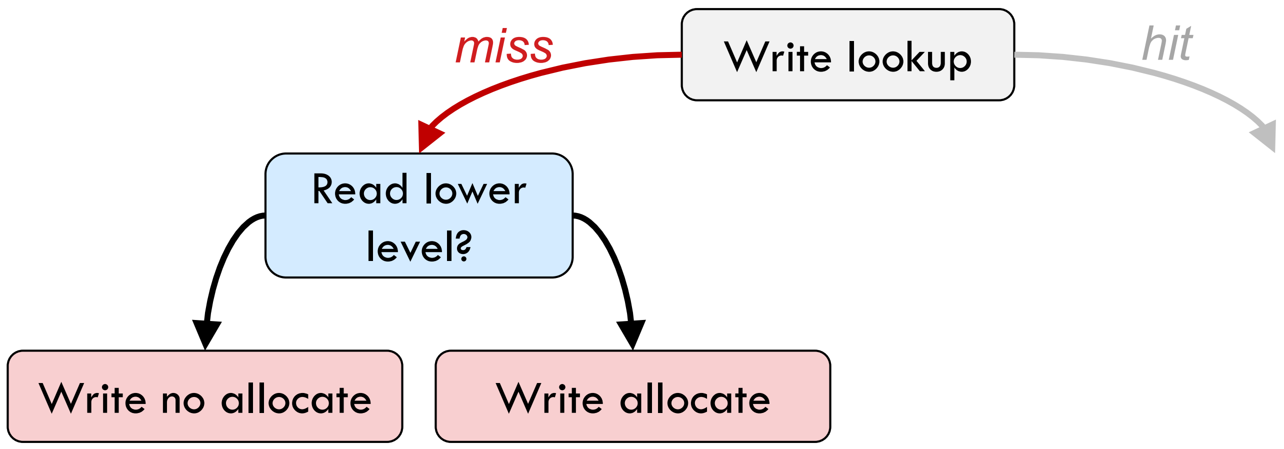

## Write (No-)Allocate

- *Write allocate*
  - allocate a cache line for the new data, and replace old line
  - just like a read miss
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- How to handle read miss after write miss?

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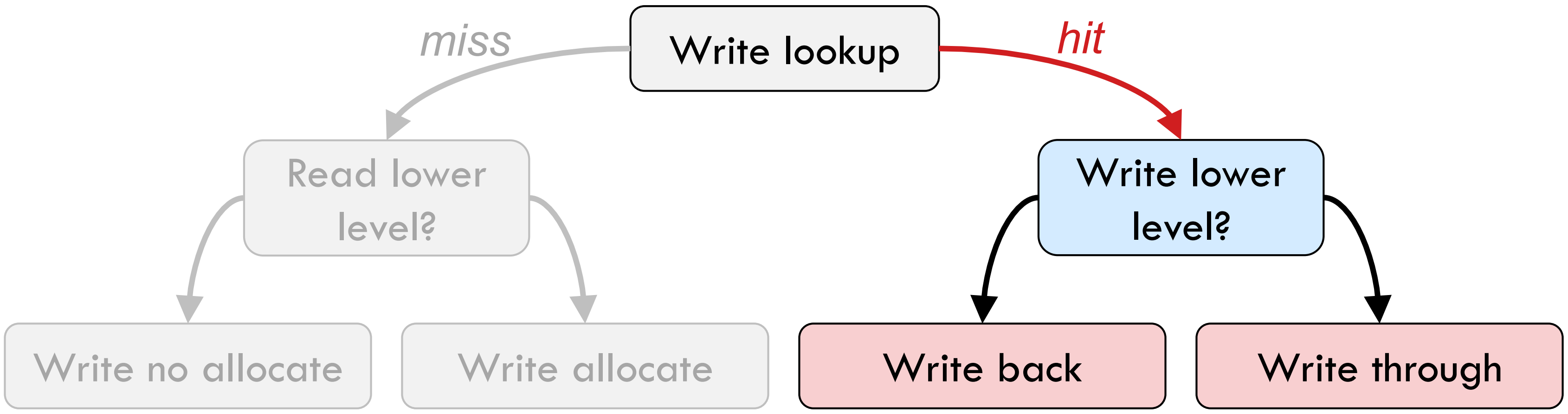
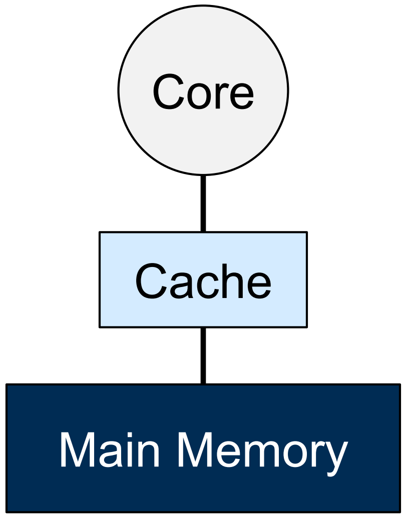


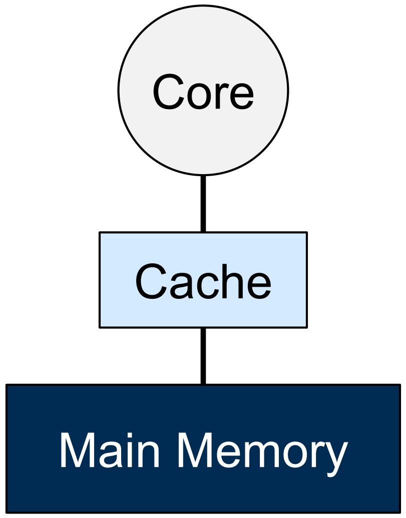
# Write back

- On a write access, write to cache only
  - write cache block to memory only when replaced from cache
  - dramatically decreases bus bandwidth usage
  - keep a bit (called the *dirty* bit) per cache block



## Write through

- Write to both cache and memory (or next level)
  - Improved miss penalty
  - More reliable because of maintaining two copies



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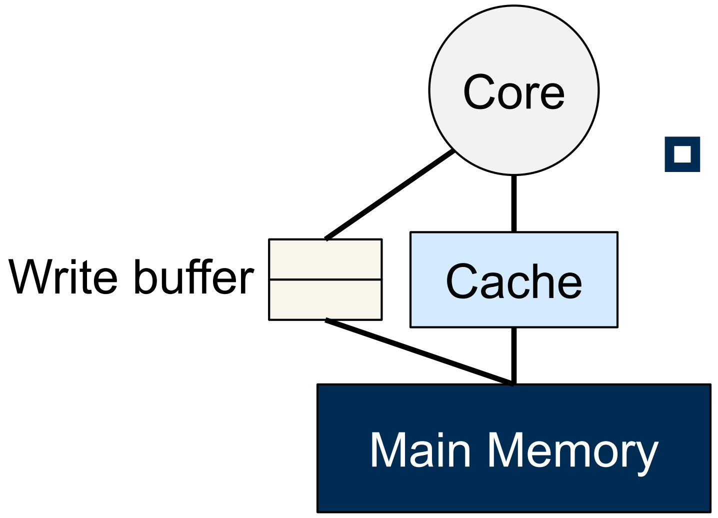

- Use write buffer alongside cache
- works fine if
  - rate of stores < 1 / DRAM write cycle
- otherwise
  - write buffer fills up
  - stall processor to allow memory to catch up

## Reducing Miss Penalty

- Some cache misses are inevitable
  - when they do happen, want to service as quickly as possible
- Other miss penalty reduction techniques
  - Multilevel caches
  - Giving read misses priority over writes
  - Sub-block placement
  - Critical word first

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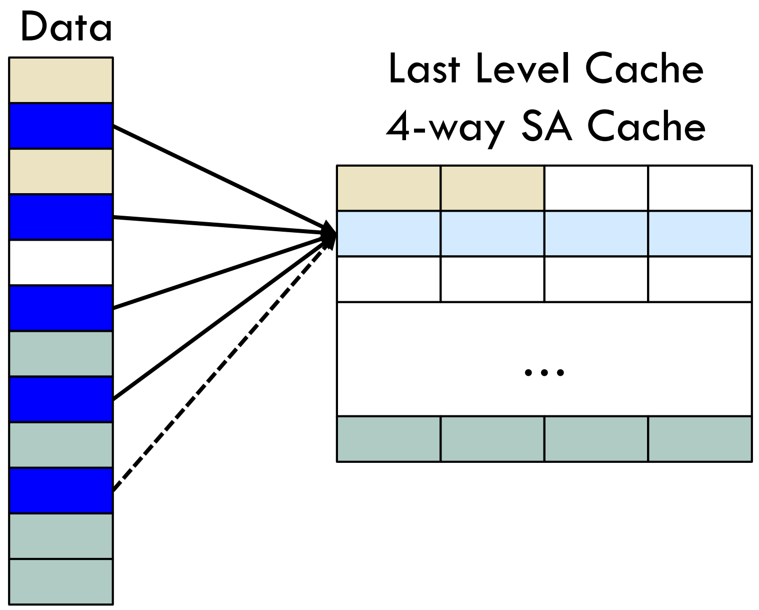
## Victim Cache

- How to reduce conflict misses
  - Larger cache capacity
  - More associativity
- Associativity is expensive
  - More hardware; longer hit time
  - More energy consumption
- Observation
  - Conflict misses do not occur in all sets
  - Can we increase associativity on the fly for sets?

## Victim Cache

- Small fully associative cache
  - On eviction, move the victim block to victim cache



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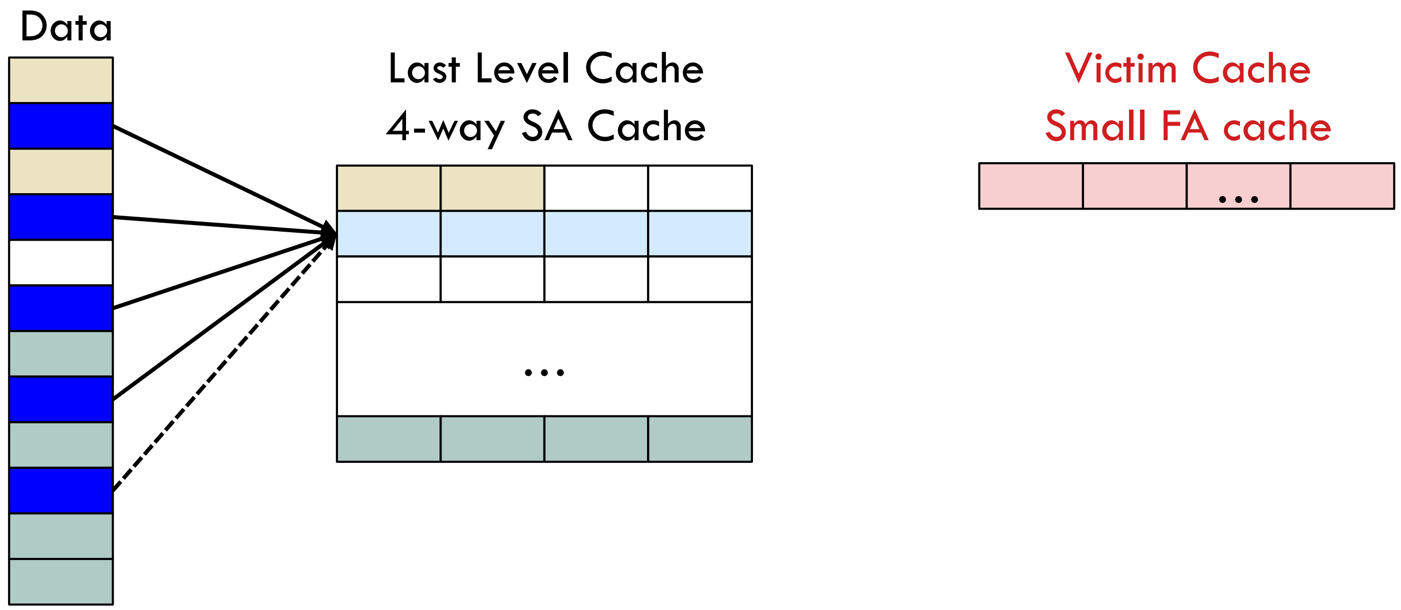

## Cache Inclusion

- How to reduce the number of accesses that miss in all cache levels?
  - Should a block be allocated in all levels?
    - Yes: inclusive cache
    - No: non-inclusive or exclusive
  - Non-inclusive: only allocated in L1
- Modern processors
  - L3: inclusive of L1 and L2
  - L2: non-inclusive of L1 (large victim cache)