OUT-OF-ORDER LOADS/STORES

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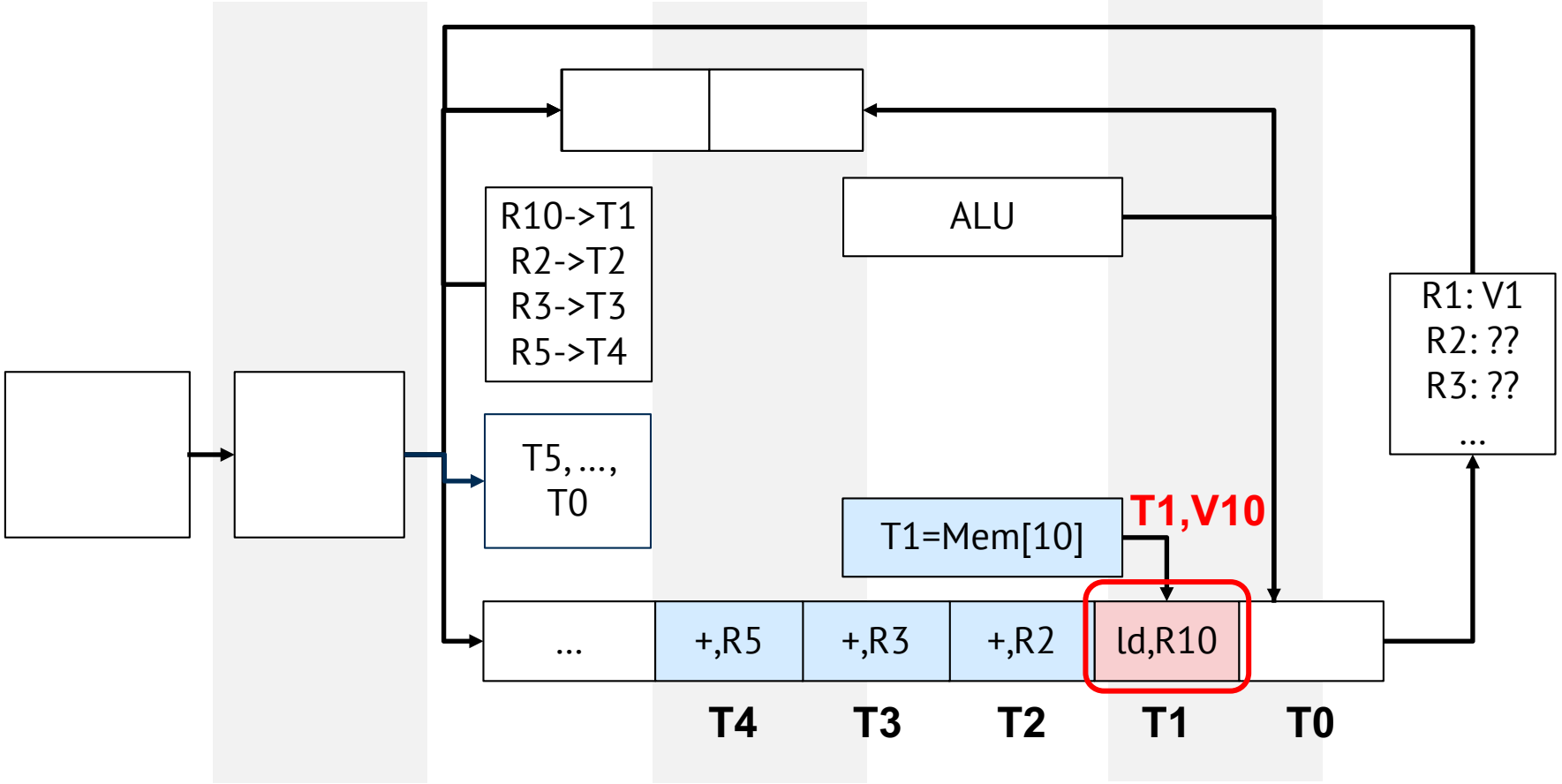
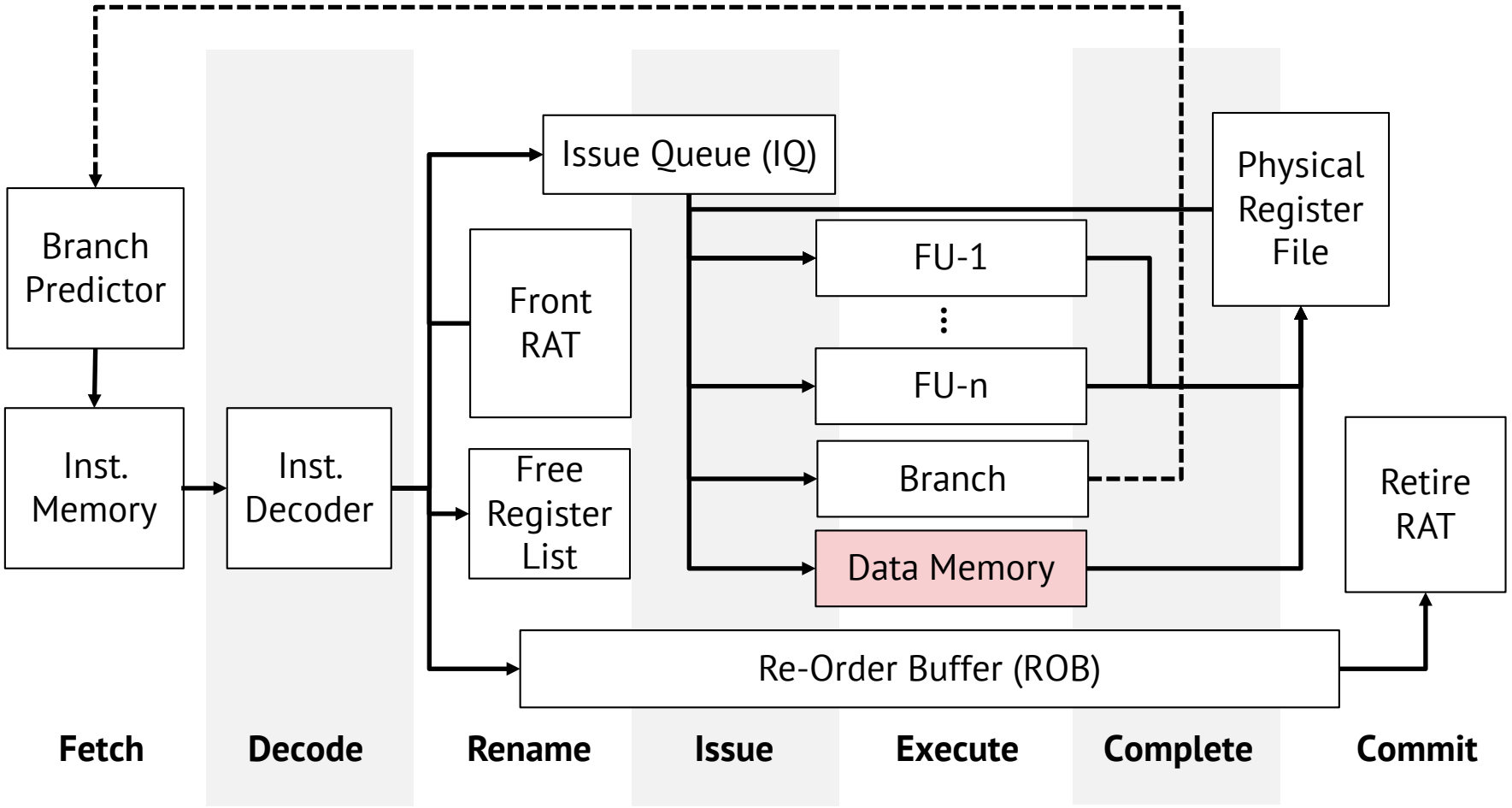
Recall: Out-of-Order Execution

- Memory accesses require long time to complete.



Loads and Stores

- Imagine multiple load/store in IQ.



Memory Data Dependence

- Can we continue executing loads/stores out-of-order?

Instructions in the issue queue

Load	R1←Mem[R2]
Load	R3←Mem[R4+8]
Store	R5→Mem[R6]
Load	R7←Mem[R8+16]
Store	R9→Mem[R10]

Memory

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  - Effective address is required for dependence check

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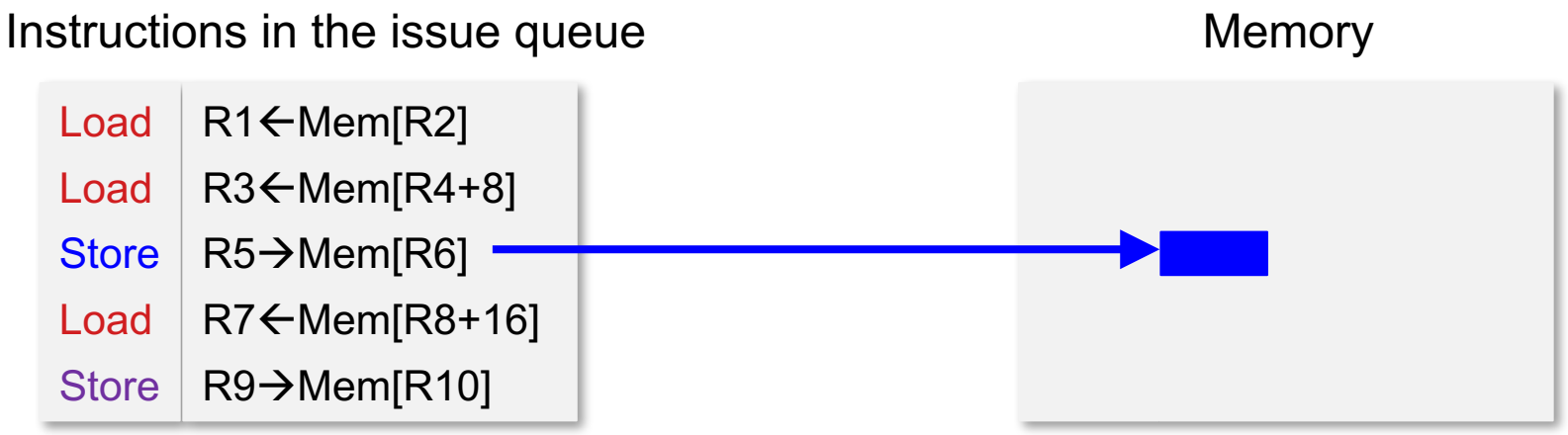

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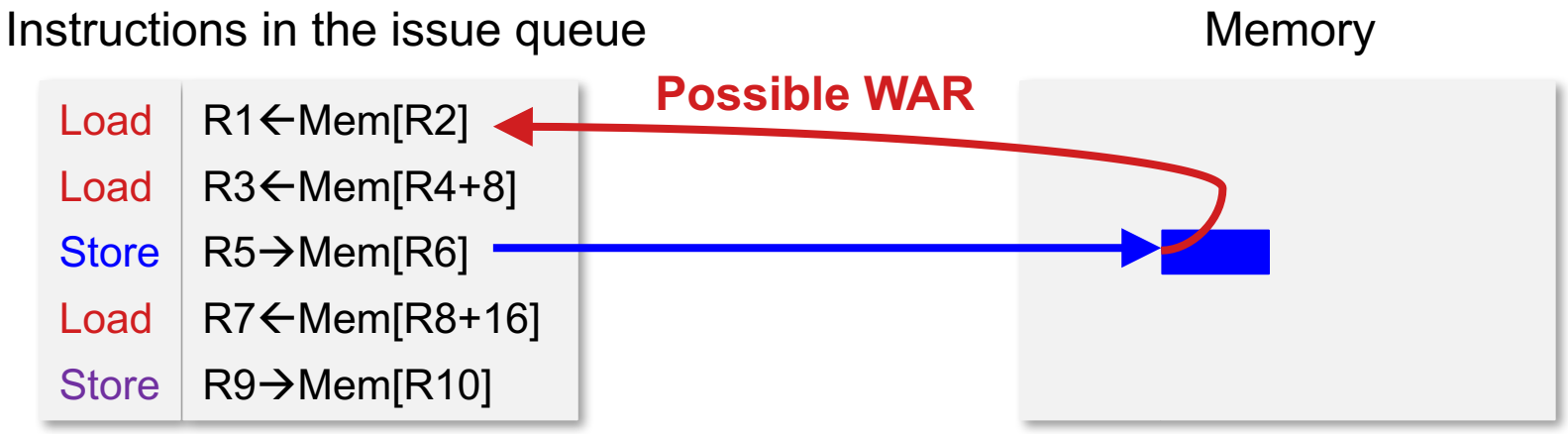

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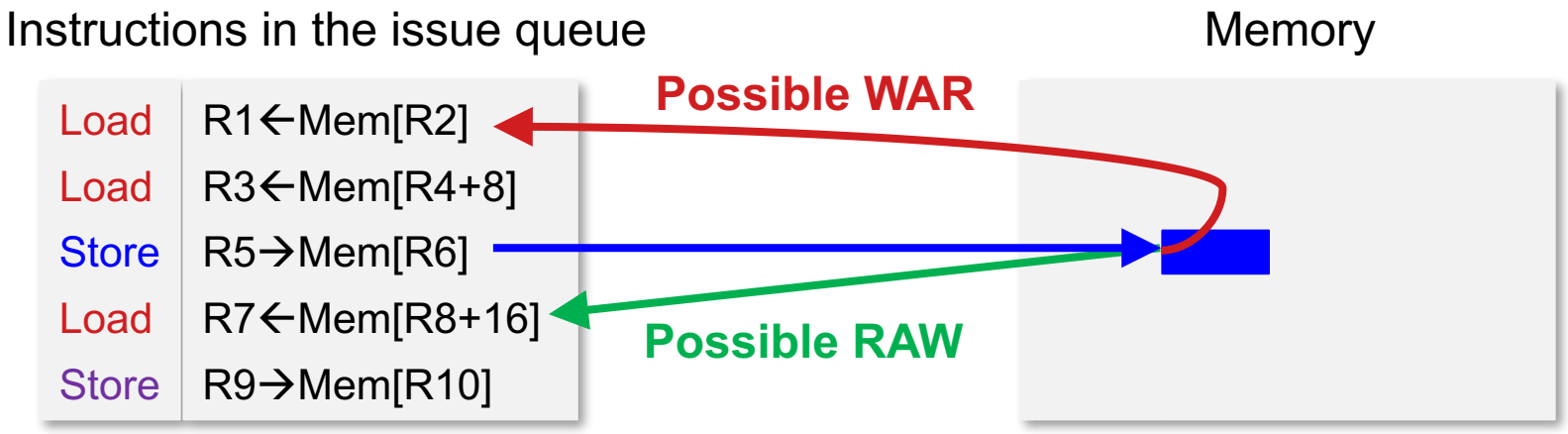

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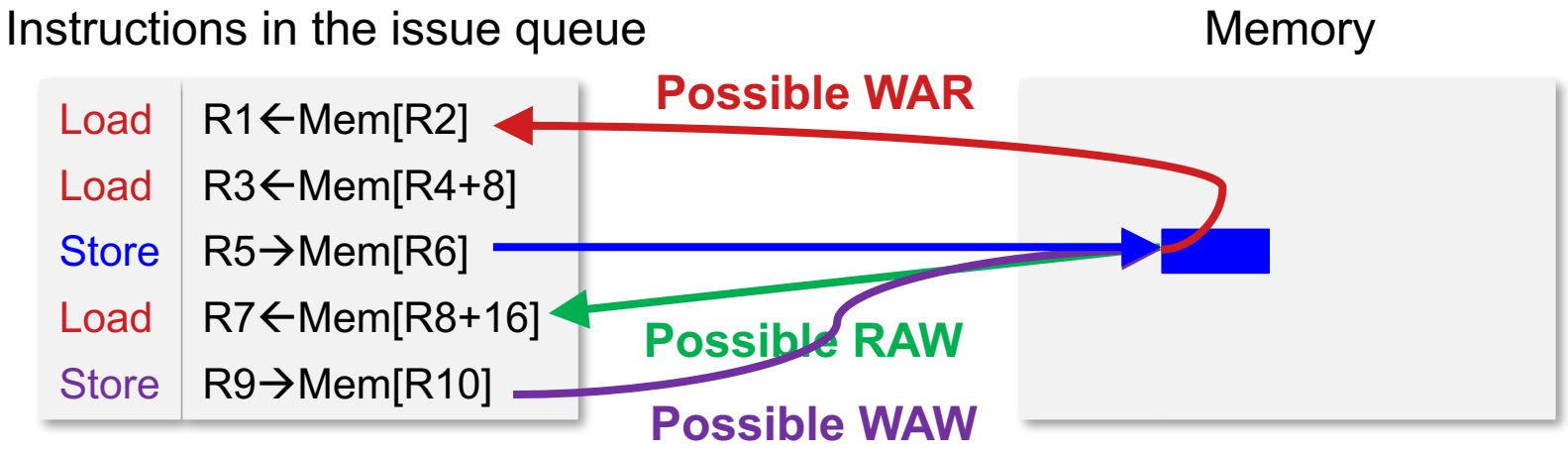

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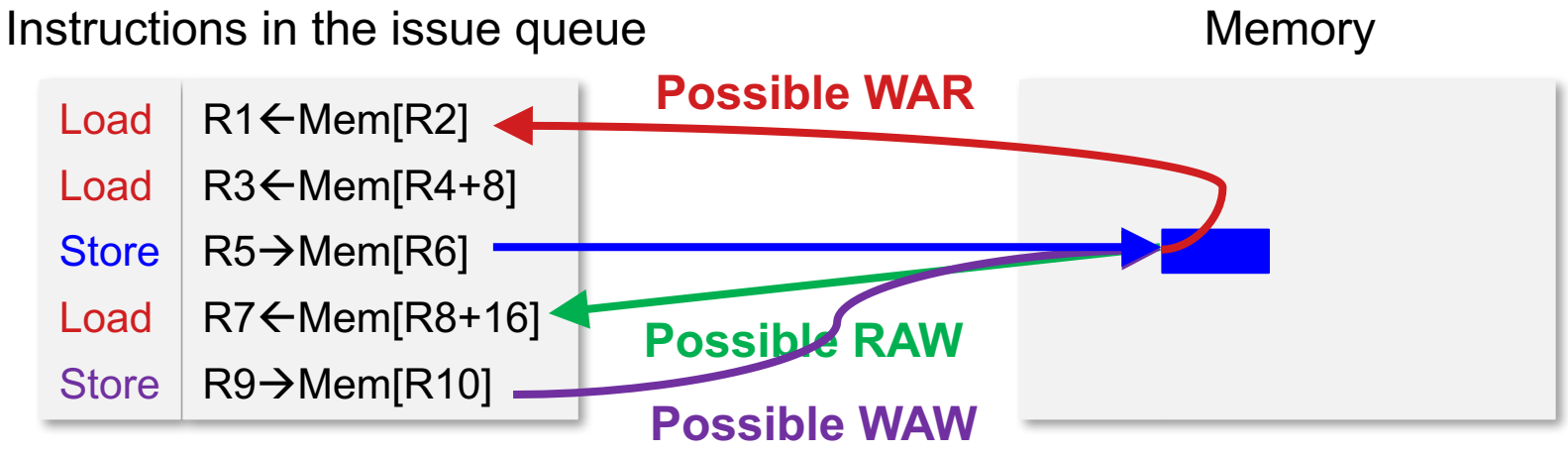
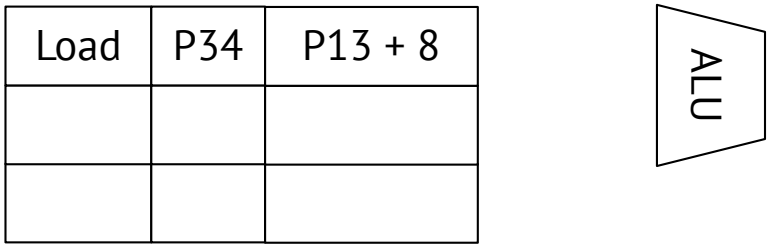


Does renaming help?

Load-Store Queue

- Dedicated queue only for load/store instructions
  - Check availability of operands every cycle
- Two steps for load/store instructions
  - Compute the effective address when register is available
  - Send the request to memory if there is no memory hazards



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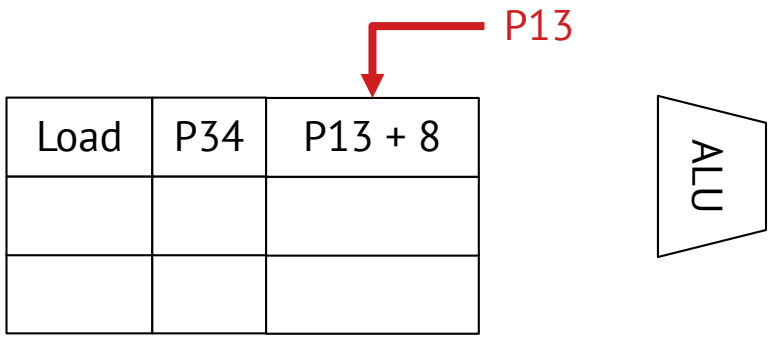

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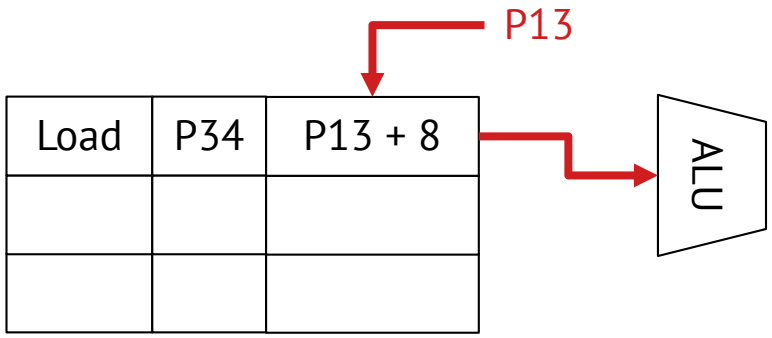

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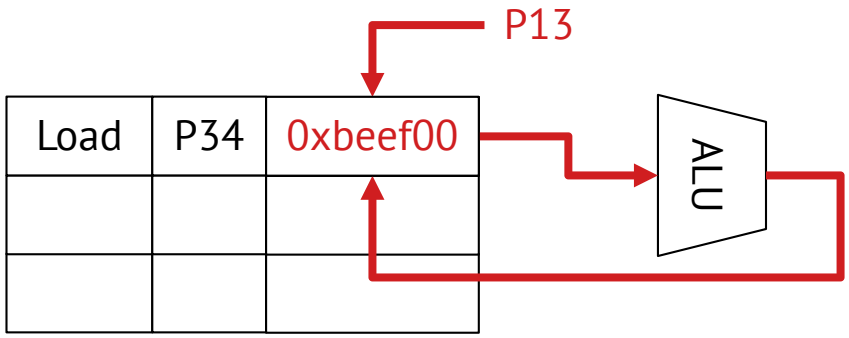
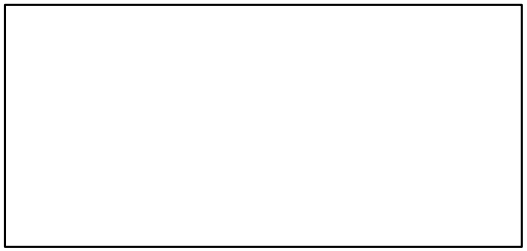


Memory Dependence Check

- Checking for RAW, WAR, and WAW hazards

Load	P34	0x12345
Load	P61	
Store	P26	
Load	P11	
Load	P29	0x12345
Store	P30	0x11111
Load	P15	0x22222
Load	P10	0x11111

1. Which load instructions can be issued?



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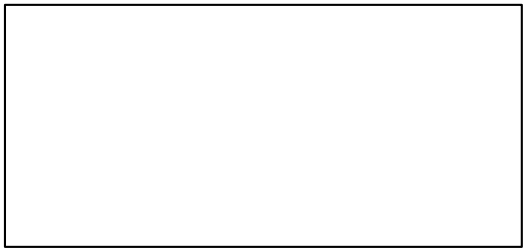
Due to RAW hazards, only those loads that are not following any unknown stores can be issued.



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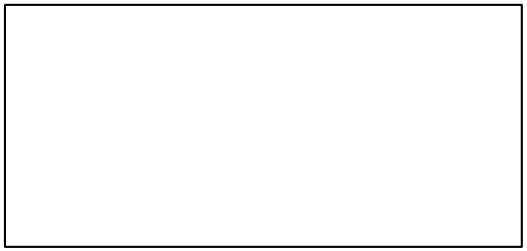
Can we bypass memory?



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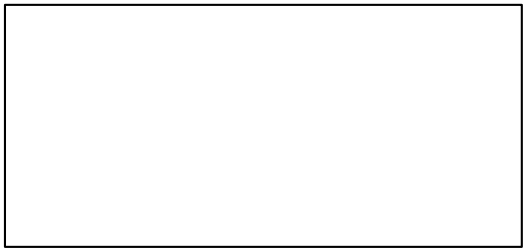
2. Which store instructions can be issued?



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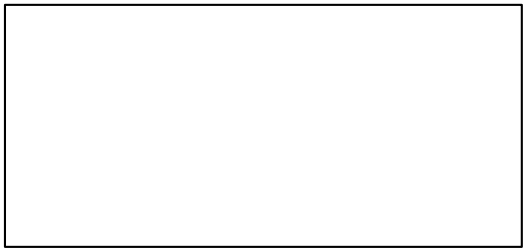
2. Which store instructions can be issued?

Due to WAW and WAR hazards, only when there is no older instructions. (why?)



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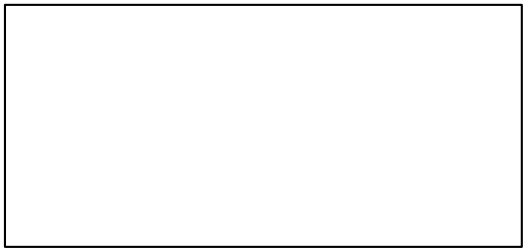
Which instructions can be issued?



Memory

Memory Dependence Prediction

- Can we predict memory dependence?

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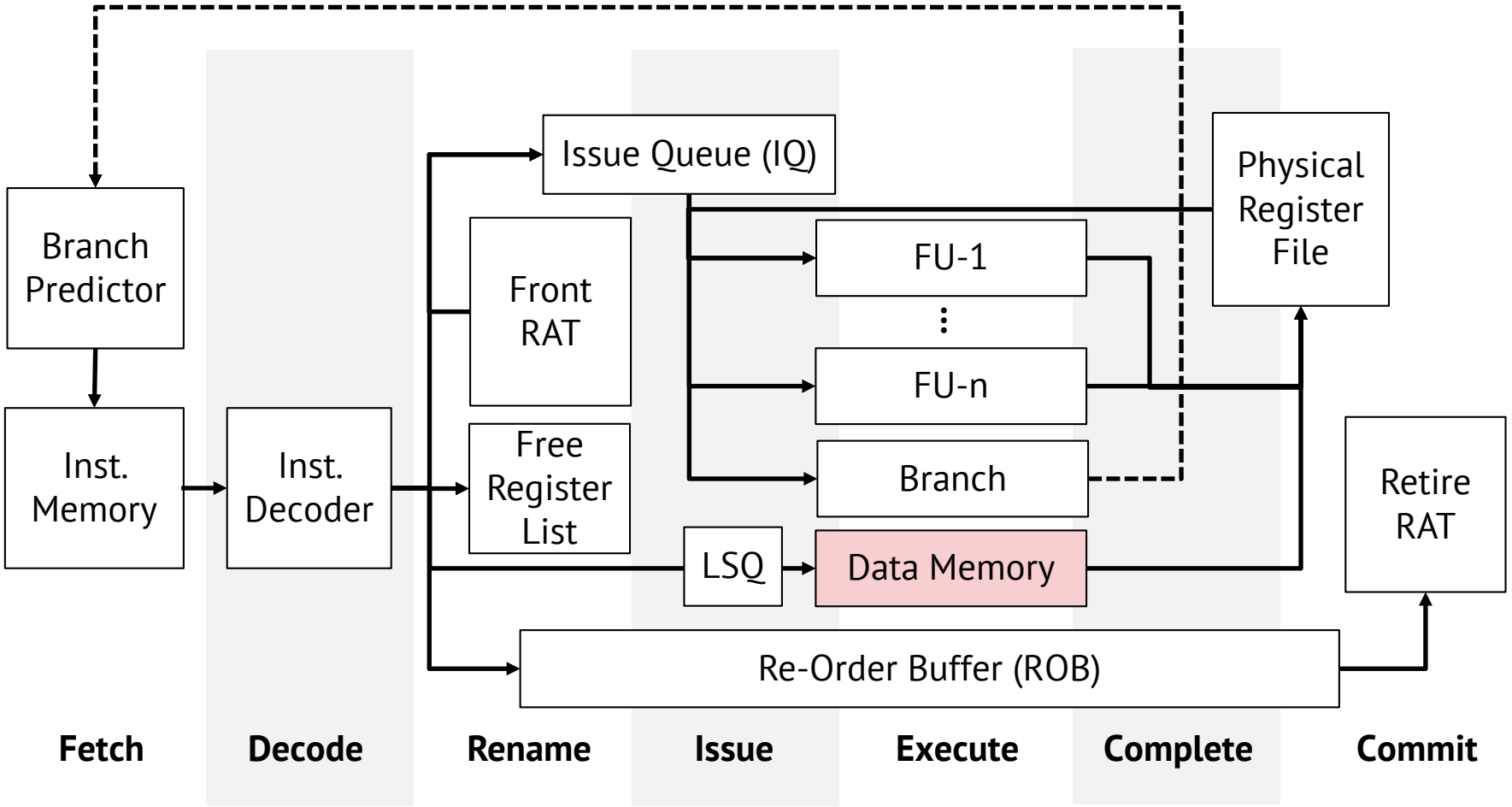
Issue/execute load instructions even if they are following unresolved stores

What if the prediction was not correct?

Out-of-order Pipeline with LSQ

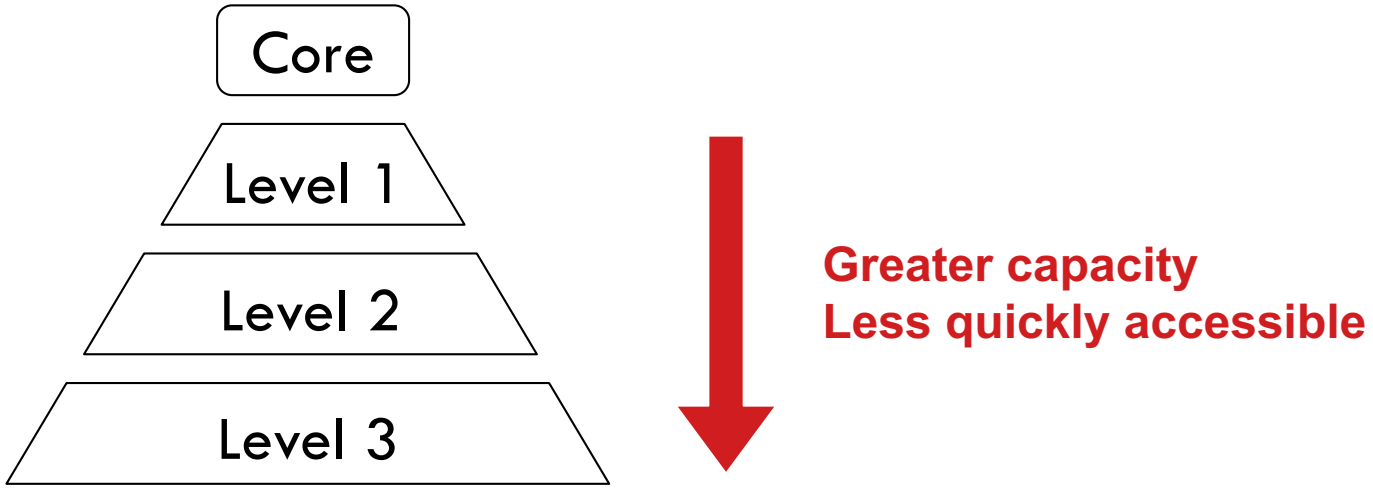
- LSQ is an extension to IQ



Memory Hierarchy

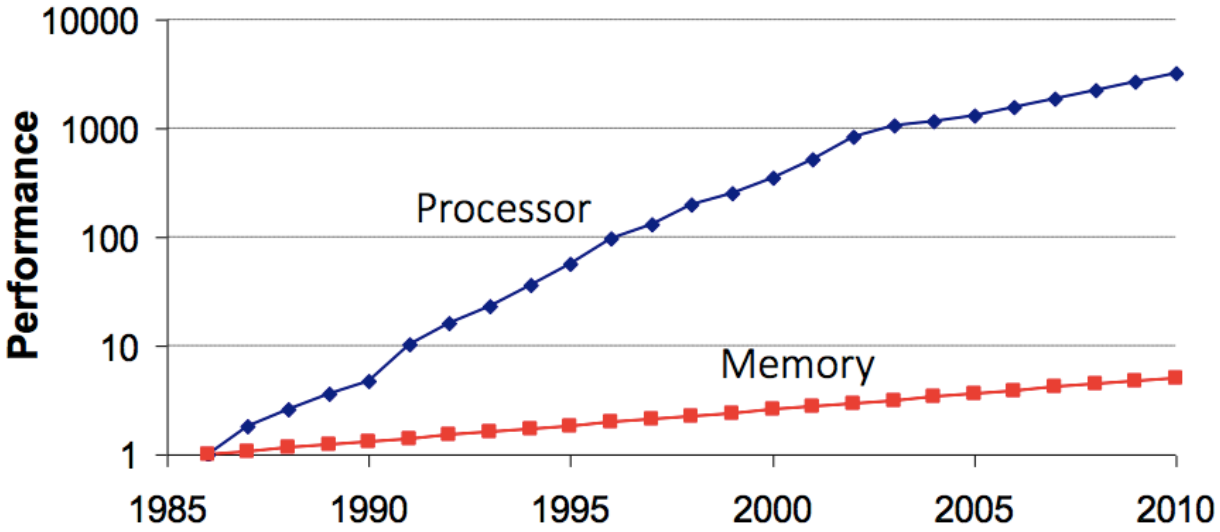
"Ideally one would desire an indefinitely large memory capacity such that any particular [...] word would be immediately available [...] We are [...] forced to recognize the possibility of constructing a hierarchy of memories, each of which has greater capacity than the preceding but which is less quickly accessible."

-- Burks, Goldstine, and von Neumann, 1946



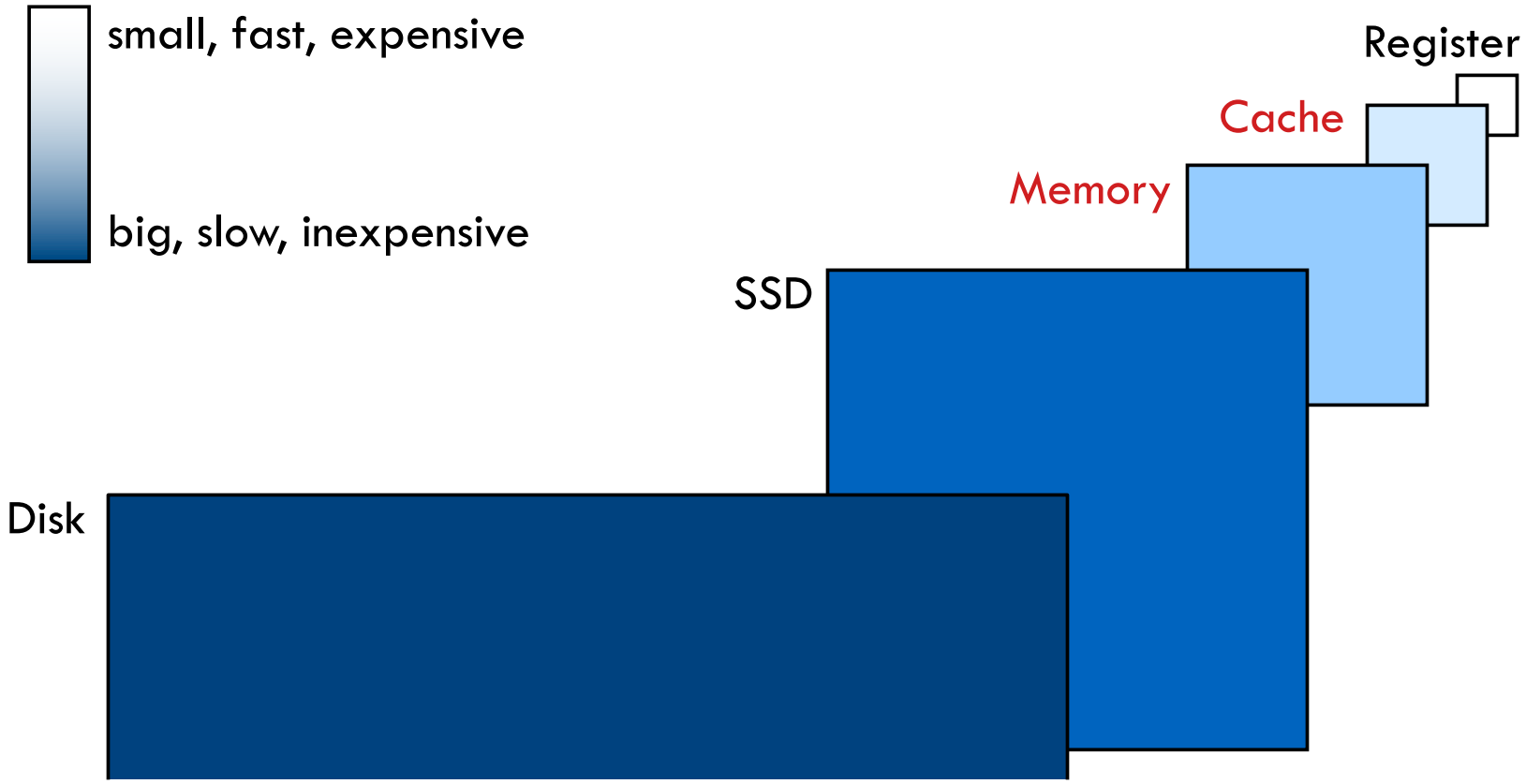
The Memory Wall

- Processor-memory performance gap increased over 50% per year
  - Processor performance historically improved ~60% per year
  - Main memory access time improves ~5% per year



Modern Memory Hierarchy

- Trade-off among memory speed, capacity, and cost

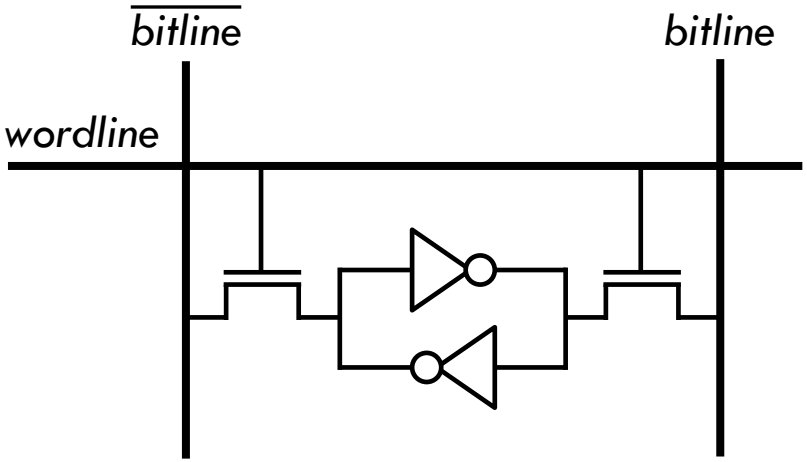


Memory Technology

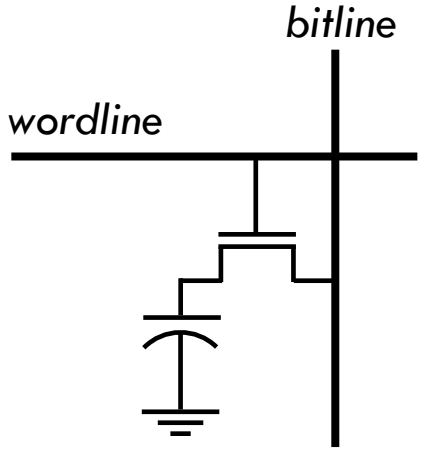
- Random access memory (RAM) technology
  - access time same for all locations (not so true anymore)
  - Static RAM (SRAM)
    - typically used for caches
    - 6T/bit; fast but – low density, high power, expensive
  - Dynamic RAM (DRAM)
    - typically used for main memory
    - 1T/bit; inexpensive, high density, low power – but slow

RAM Cells

- 6T SRAM cell
  - internal feedback maintains data while power on



- 1T-1C DRAM cell
  - needs refresh regularly to preserve data



Processor Cache

- Occupies a large fraction of die area in modern microprocessors

3-3.5 GHz
~$1000 2014)

Source: Intel Core i7

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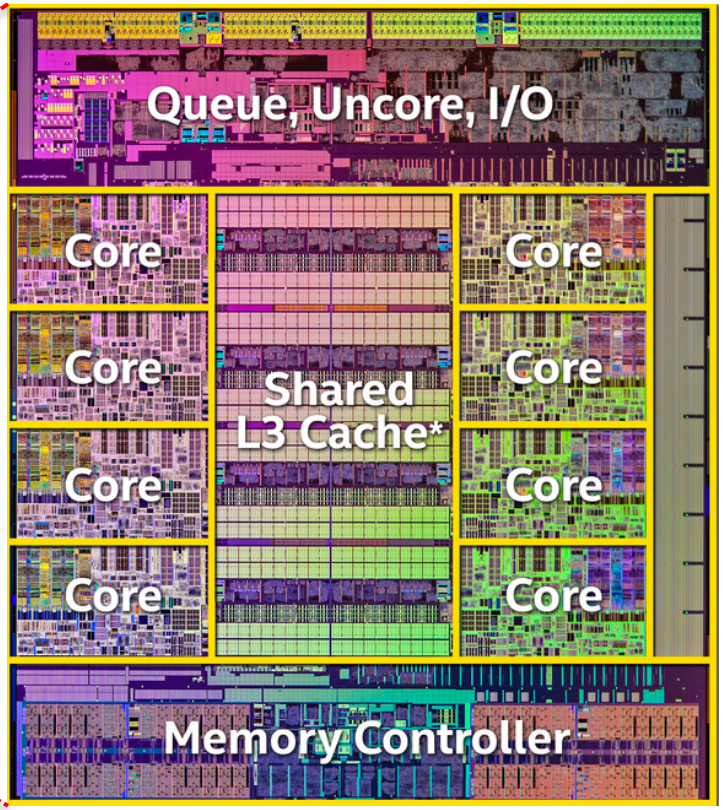
20MB of cache



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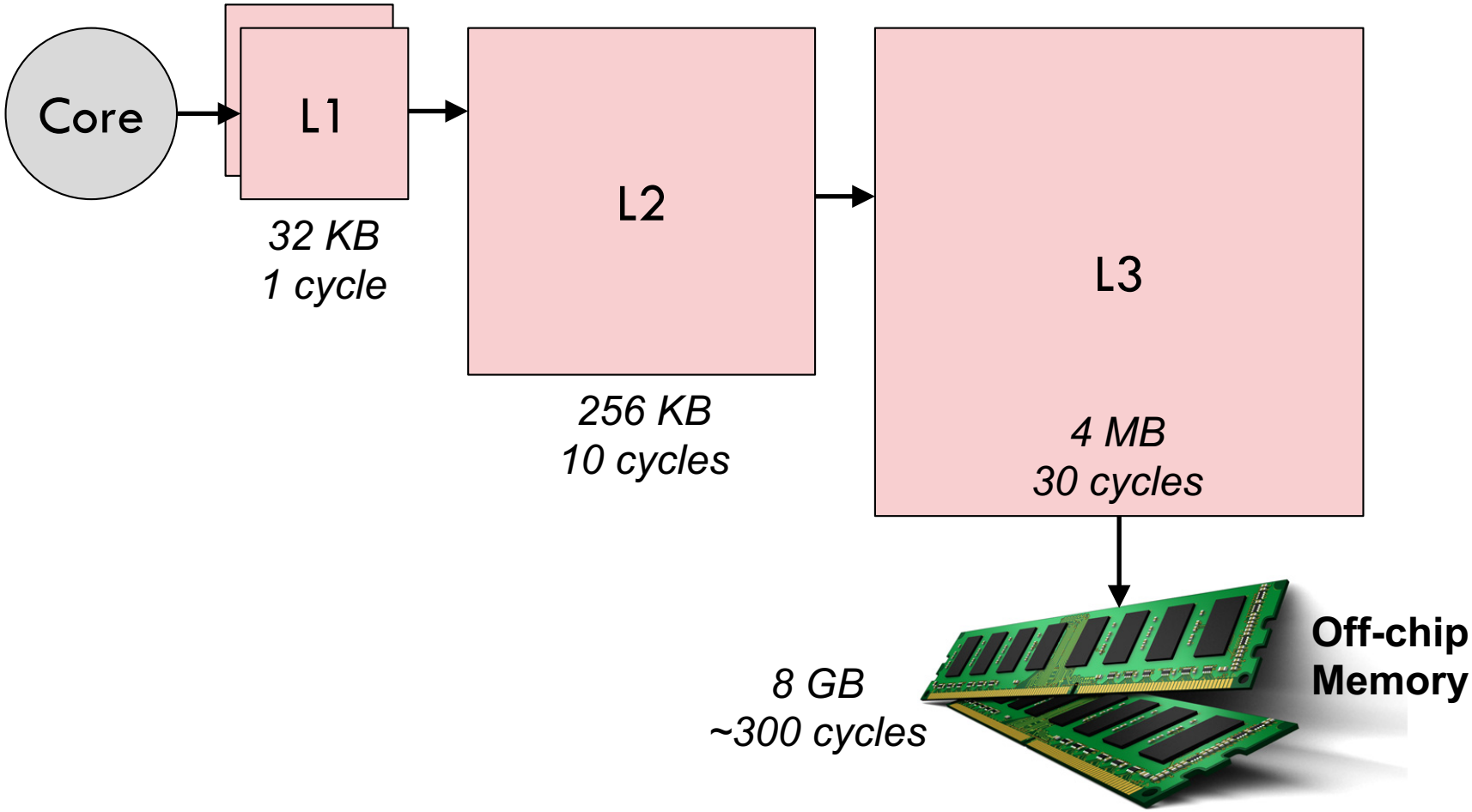
Cache Hierarchy

- Example three-level cache organization



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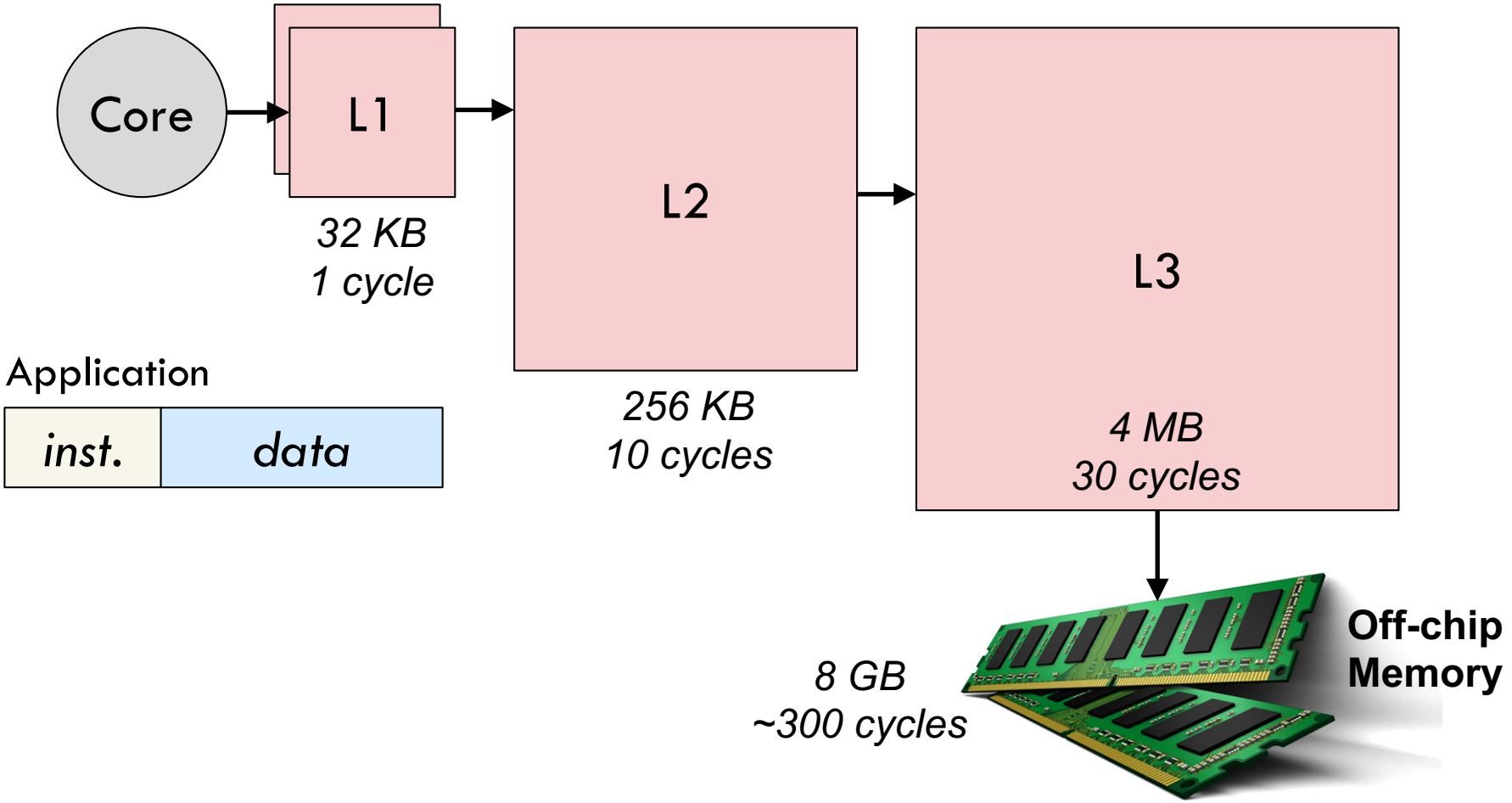

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