MEMORY SYSTEM

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Overview

- This lecture
 - Cache miss types
 Cold, capacity, and conflict
 Replacement policies
 Ideal, LRU, and MRU

- Start by measuring miss rate with an ideal cache
 - 1. ideal is fully associative and infinite capacity
 - 2. then reduce capacity to size of interest
 - 3. then reduce associativity to degree of interest

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 How to improve
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3. Conflict 1. Cold (compulsory) 2. Capacity Cache is smaller Cold start: first Set size is smaller than the program access to block than mapped How to improve data mem. locations How to improve large blocks How to improve ○ prefetching ○ large cache ○ large cache

○ more assoc.

Miss Rates: Example Problem

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L1 miss rates
3,000/100,000 = 3%
L2 miss rates
1,500/3,000 = 50%

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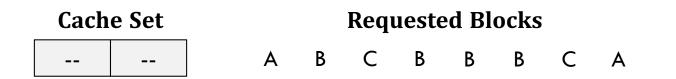
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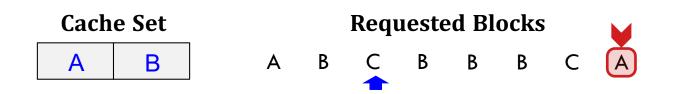
Which one is better?

- □ Which block to replace on a miss?
 - Only one candidate in direct-mapped cache
 - Multiple candidates in set/fully associative cache

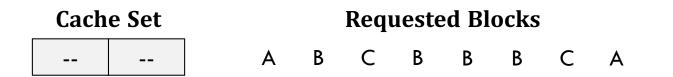
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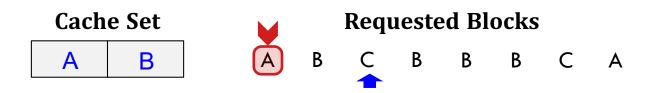
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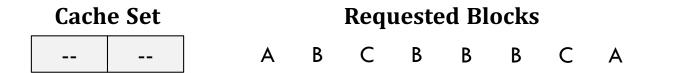
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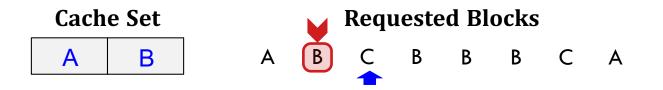
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- Random replacement
 - hardware randomly selects a cache block to replace

Example Problem

Blocks A, B, and C are mapped to a single set with only two block storages; find the miss rates for LRU and MRU policies.

2. A, A, B, B, C, C, A, B, C

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- 1. A, B, C, A, B, C, A, B, C
 LRU : 100%
 MRU : 66%
- 2. A, A, B, B, C, C, A, B, C
 LRU: 66%
 MRU: 44%