MEMORY SYSTEM

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Overview

- This lecture
  - Cache terminologies
  - Cache performance
  - Cache addressing

Cache Terminology

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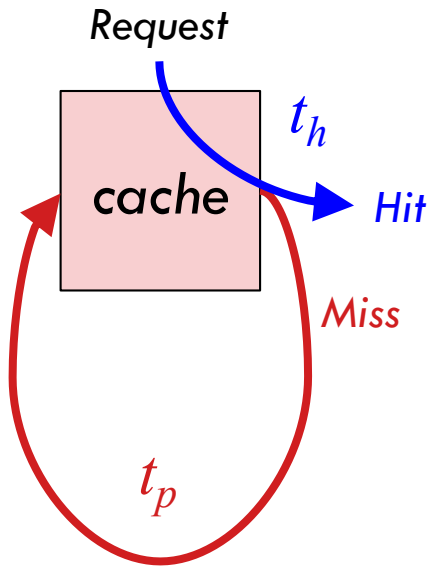
hit time << miss penalty

Cache Performance

- Average Memory Access Time (AMAT)

Outcome	Rate	Access Time
Hit	r_h	t_h
Miss	r_m	$t_h + t_p$



$$AMAT = r_h t_h + r_m (t_h + t_p)$$

$$r_h = 1 - r_m$$

$$AMAT = t_h + r_m t_p$$

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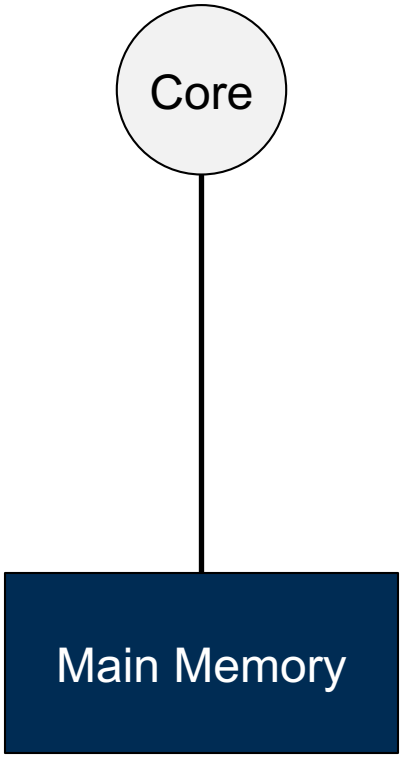
AMAT = 2 + 0.1x200 = 22 cycles

Summary: Cache Performance

- Bridging the processor-memory performance gap



Main memory access time: 300 cycles

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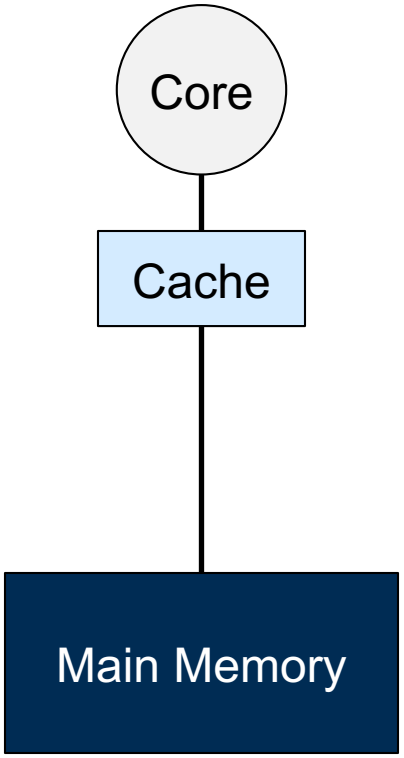

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Cache

- L1: 2 cycles hit time; 60% hit rate

What is the average mem access time?

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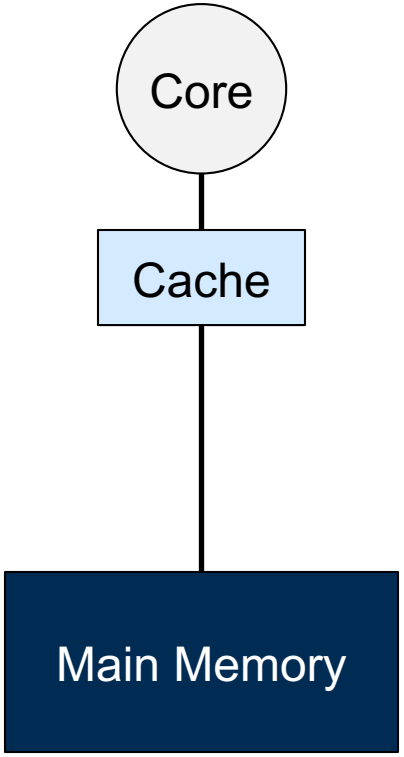


Main memory access time: 300 cycles

Cache

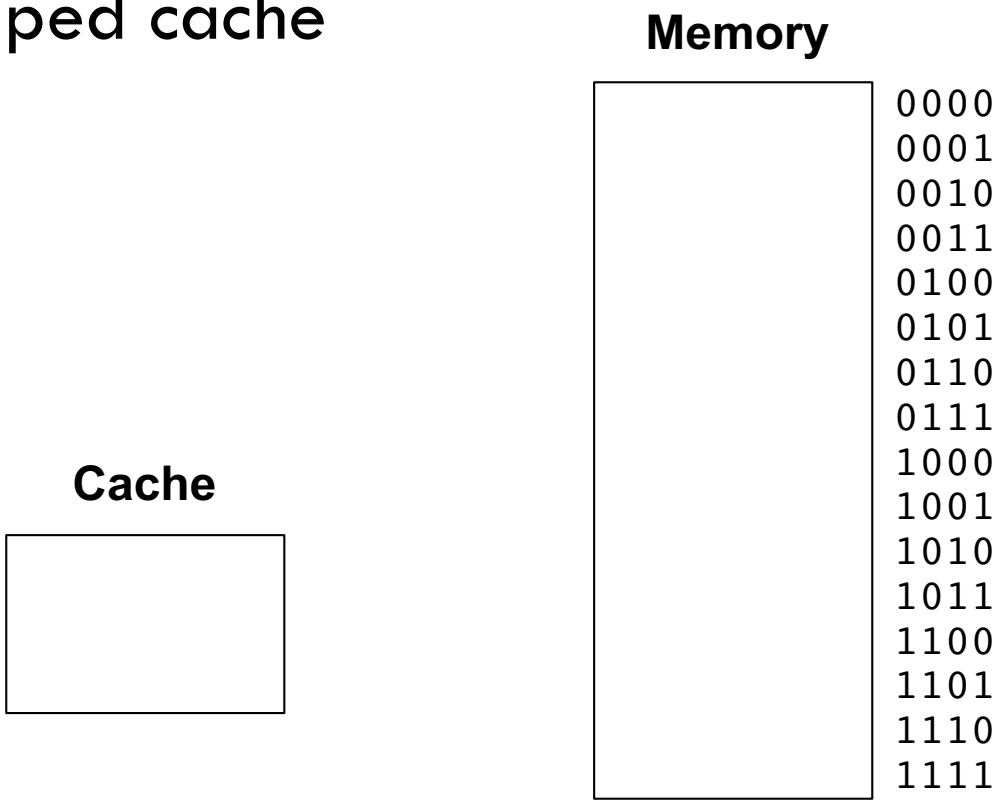
- L1: 2 cycles hit time; 60% hit rate

What is the average mem access time?

$$AMAT = t_h + r_m\, t_p$$
$$= 2 + 0.4 \times 300$$
$$= 122$$

Cache Addressing

- Instead of specifying cache address we specify main memory address
- Simplest: direct-mapped cache



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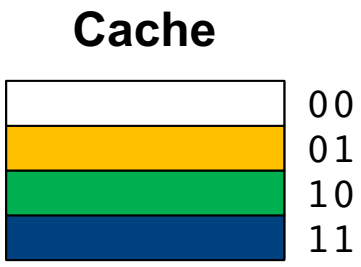

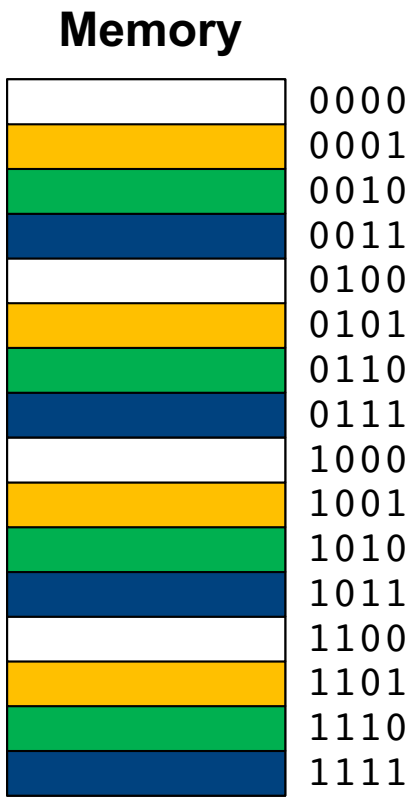

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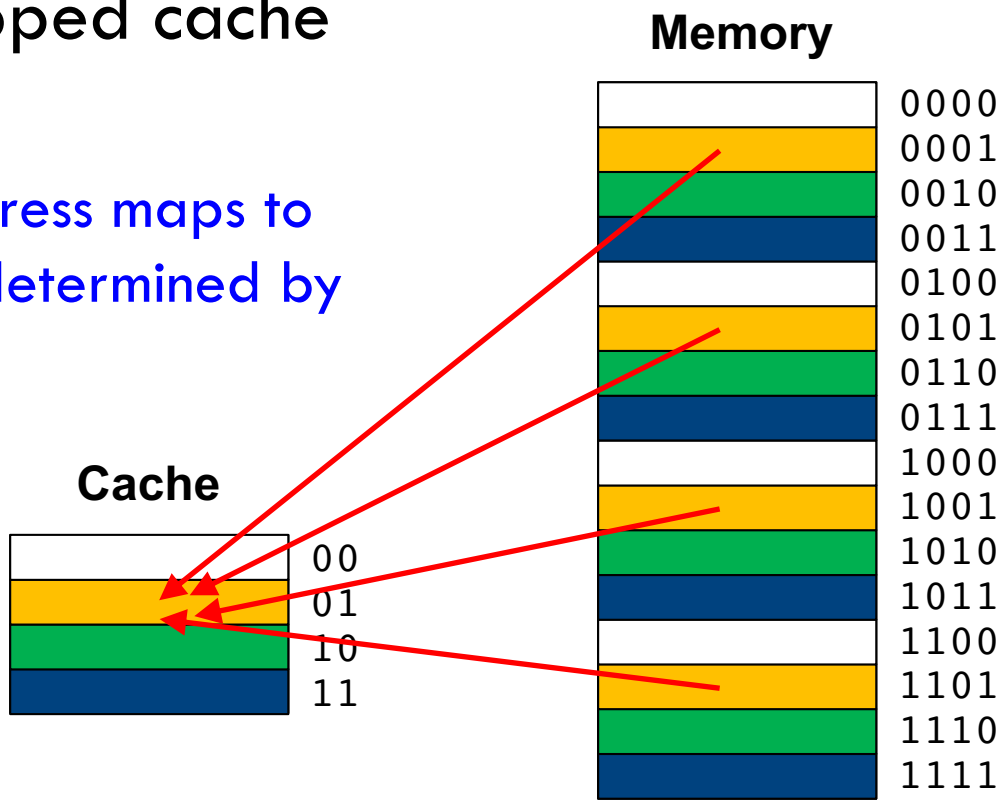
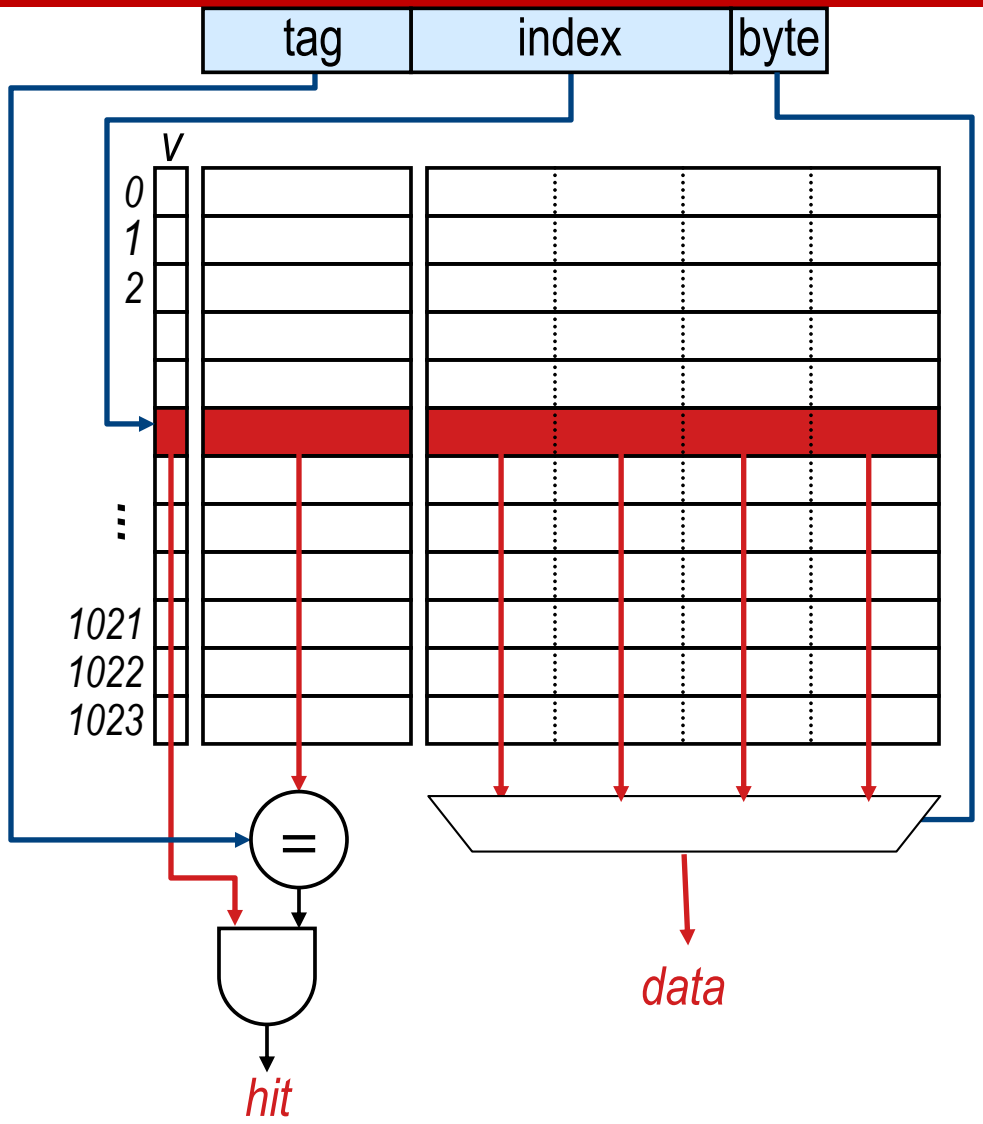
How to exactly specify which blocks are in the cache?



Direct-Mapped Lookup

- Byte offset: to select the requested byte
- Tag: to maintain the address
- Valid flag (v): whether content is meaningful
- Data and tag are always accessed



Example Problem

- Find the size of tag, index, and offset bits for an 8MB, direct-mapped L3 cache with 64B cache blocks. Assume that the processor can address up to 4GB of main memory.

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- $4GB = 2^{32}$ B → address bits = 32
- $64B = 2^{6}$ B → byte offset bits = 6
- $8MB/64B = 2^{17}$ → index bits = 17
- tag bits = 32 – 6 – 17 = 9