

INTRODUCTION AND LOGISTICS

Mahdi Nazm Bojnordi

Assistant Professor

School of Computing

University of Utah

Overview

- This lecture
 - ▣ Instructor
 - ▣ Teaching assistants
 - ▣ Course resources and requirements
 - ▣ Academic integrity
 - ▣ Computer organization
 - ▣ Trends and challenges

Instructor

- Mahdi Nazm Bojnordi
 - ▣ Assistant Professor of School of Computing
 - ▣ PhD degree in Electrical Engineering
 - ▣ Personal webpage
 - <http://www.cs.utah.edu/~bojnordi/>
- Research in Computer Architecture
 - ▣ Novel Memory Technologies
 - ▣ Energy-Efficient Hardware Accelerators
 - ▣ Research Lab. (MEB 3383)
 - **Open positions for research are available! (email me)**
- Class webpage (in addition to Canvas)
 - ▣ <http://www.cs.Utah.edu/~bojnordi/classes/3810/f20/>



Webpage

□ Please visit online

CS/ECE 3810: Computer Organization

Course Information

- † Instructor: Mahdi Nazm Bojnordi, email: lastname@cs.utah.edu, office hours: email me for appointment, MEB 3418
- † Teaching Assistants: Ananth Prasad, office hours: TBD; Paarth Lakhani, office hours: TBD; Abishek Krishnan, office hours: TBD; Saivamshi Dobbali, office hours: TBD; Trisha gangadhar, office hours: TBD
- † TAs will be available via Zoom during their office hours. Please use the [TA Queue](#) to get in line.
- † Pre-Requisite: Knowledge of structured programming languages such as C/Java
- † Textbook: Computer Organization and Design - The Hardware/Software Interface - 5th Edition, David Patterson and John Hennessy
- † Canvas is the main venue for class announcements, homework assignments, and discussions.

Important Policies

Please refer to the [College of Engineering Guidelines](#) for disabilities, add, drop, appeals, etc. Notice that we have zero tolerance for cheating; as a result, please read the [Policy Statement on Academic Misconduct](#), carefully. Also, you should be aware of the [SoC Policies and Guidelines](#).

Class rosters are provided to the instructor with the student's legal name as well as "Preferred first name" (if previously entered by you in the Student Profile section of your CIS account). While CIS refers to this as merely a preference, I will honor you by referring to you with the name and pronoun that feels best for you in class, on papers, exams, group projects, etc. Please advise me of any name or pronoun changes (and please update CIS) so I can help create a learning environment in which you, your name, and your pronoun will be respected.

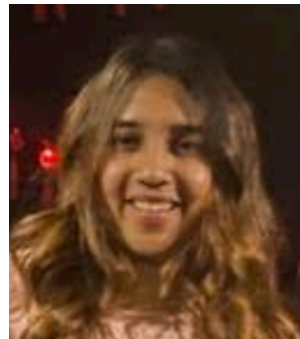
Special Needs

The University of Utah seeks to provide equal access to its programs, services and activities for people with disabilities. If you will need accommodations in the class, reasonable prior notice needs to be given to the Center for Disability Services, 162 Olpin Union Building, 581-5020 (V/TDD). CDS will work with you and the instructor to make arrangements for accommodations. All written information in this course can be made available in alternative format with prior notification to the Center for Disability Services.

Cheating policy

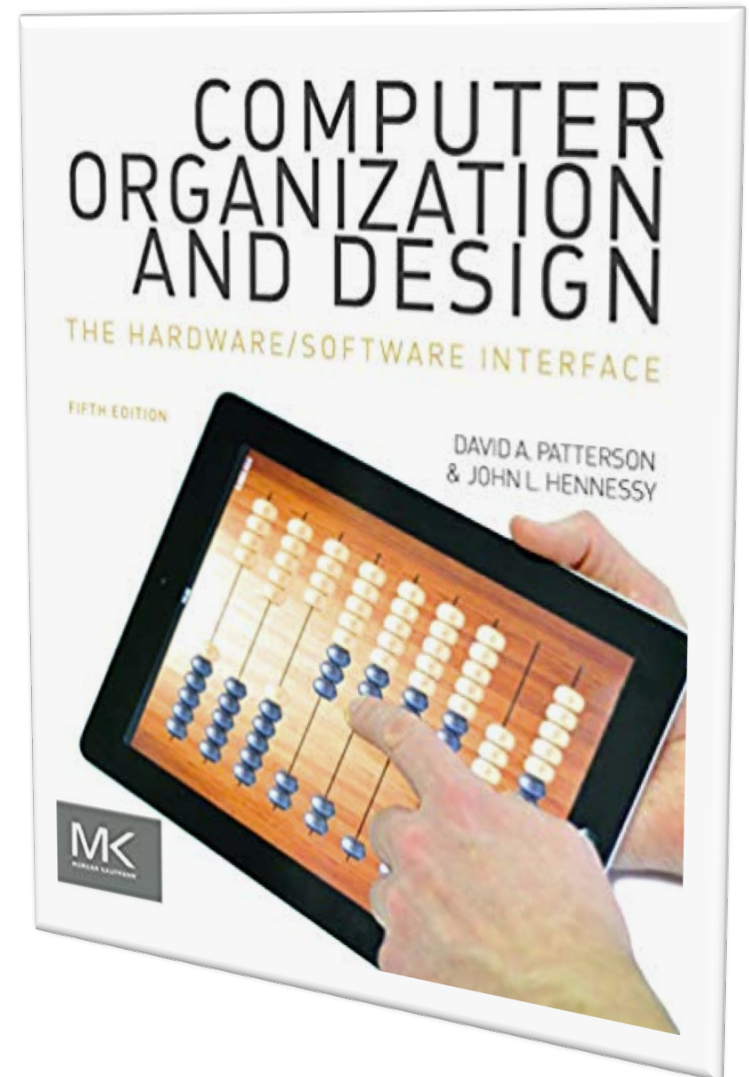
Teaching Assistants

- Ananth Krishna Prasad
 - ▣ Email: u1210117@utah.edu
- Abishek Krishnan
 - ▣ Email: u1261980@utah.edu
- Paarth Lakhani
 - ▣ Email: u0936913@utah.edu
- SaiVamshi Dobbali
 - ▣ Email: u1266122@utah.edu
- Trisha Gangadhar
 - ▣ Email: u1302432@utah.edu



Resources and Requirements

- Textbook: Computer Organization and Design - The Hardware/Software Interface - 5th Edition, David Patterson and John Hennessy
- Pre-requisite: Knowledge of structured programming languages such as C/Java



Course Expectation

- We use Canvas for homework submissions, grades, and homework announcements.
- Grading

	Fraction	Notes
Assignments	30%	Homework assignments
Midterm Exam	30%	Tuesday, October 13st
Final Exam	30%	Monday, December 7th
Quizzes	10%	Questions in Canvas

Homework Assignments

- Homework assignments will be released on Canvas; all submissions must be made through Canvas.
- Only those submissions made before midnight will be accepted.
- Any late submission will be considered as no submission.
- You may skip 1 out of 11 (= we drop one HW with the least score).

	Release Date	Submission Deadline
Homework 1	09/02	09/09
Homework 2	09/09	09/16
Homework 3	09/16	09/23
Homework 4	09/23	09/30
Homework 5	09/30	10/07
Homework 6	10/07	10/13
Homework 7	10/19	10/26
Homework 8	10/26	11/02
Homework 9	11/09	11/16
Homework 10	11/16	11/23
Homework 11	11/23	12/02

Quizzes

- Quizzes comprising multiple-choice, true/false, yes/no, and fill-in-the blank questions will be released on Canvas.
- Read the relevant chapters of the textbook and review the lectures before taking each quiz. **Only one attempt is allowed for each quiz during the specific dates below.**

	Lectures	Release Date	Submission Deadline
Quiz 1	1-3	08/31	09/02
Quiz 2	4,5	09/09	09/11
Quiz 3	6,7	09/16	09/18
Quiz 4	8,9	09/23	09/25
Quiz 5	10,11	09/30	10/02
Quiz 6	12,13	10/07	10/19
Quiz 7	14,15	10/19	10/21
Quiz 8	16,17	10/26	10/28
Quiz 9	18-21	11/09	11/11
Quiz 10	22,23	11/16	11/18
Quiz 11	24,25	11/23	12/04

Academic Integrity

- Do NOT cheat!!
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- For more information, please refer to the important policies on the class webpage.

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Working with others on assignments is a good way to learn the material and is encouraged. However, there are limits to the degree of cooperation that is permitted. Students may discuss among themselves the meaning of homework problems and possible approaches to solving them. Any written portion of an assignment, however, is to be done strictly on an individual basis. **BOTTOM LINE:** You may not copy from another student or from any other source, and you may not allow another student to copy your work!! Any violation of the above is considered to be cheating and will result in a reduced or a failing grade in the class. TAs will be on the lookout for solution sets that appear very similar. Also, if your class rank in the assignments is significantly different from your class rank in the exams, only your rank in the exams will count towards your grade.

Why CS/ECE 3810?

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- Understand the technology trends and recent developments for future computing?
- ...

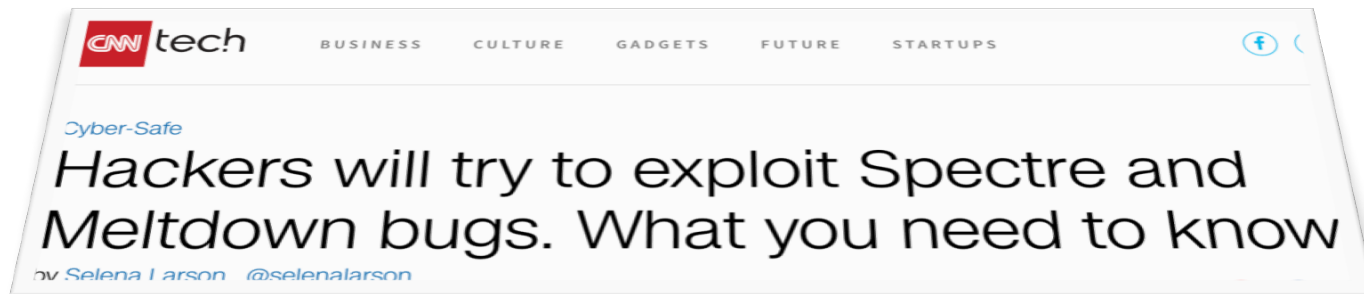
Why study computer organization?

- Do the conventional computers last forever?
 - ▣ New challenges
 - ▣ New forms of computing



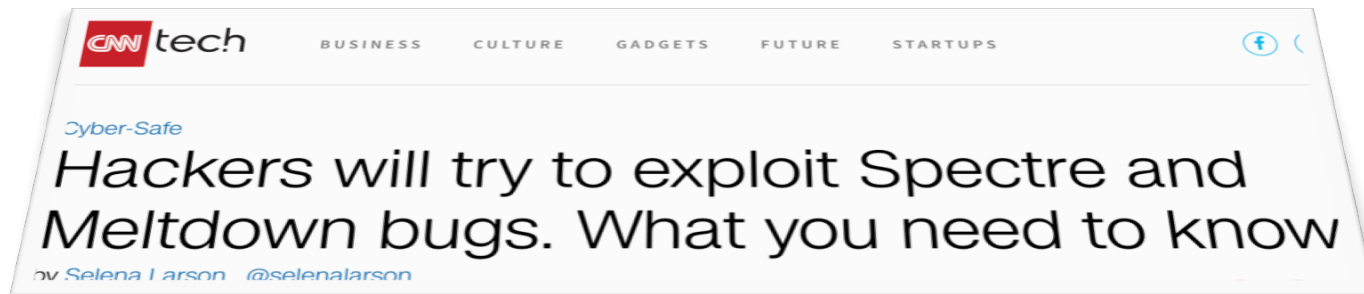
Why study hardware?

- Better understanding of today's computing problems
 - ▣ Security flaw: Spectre and Meltdown



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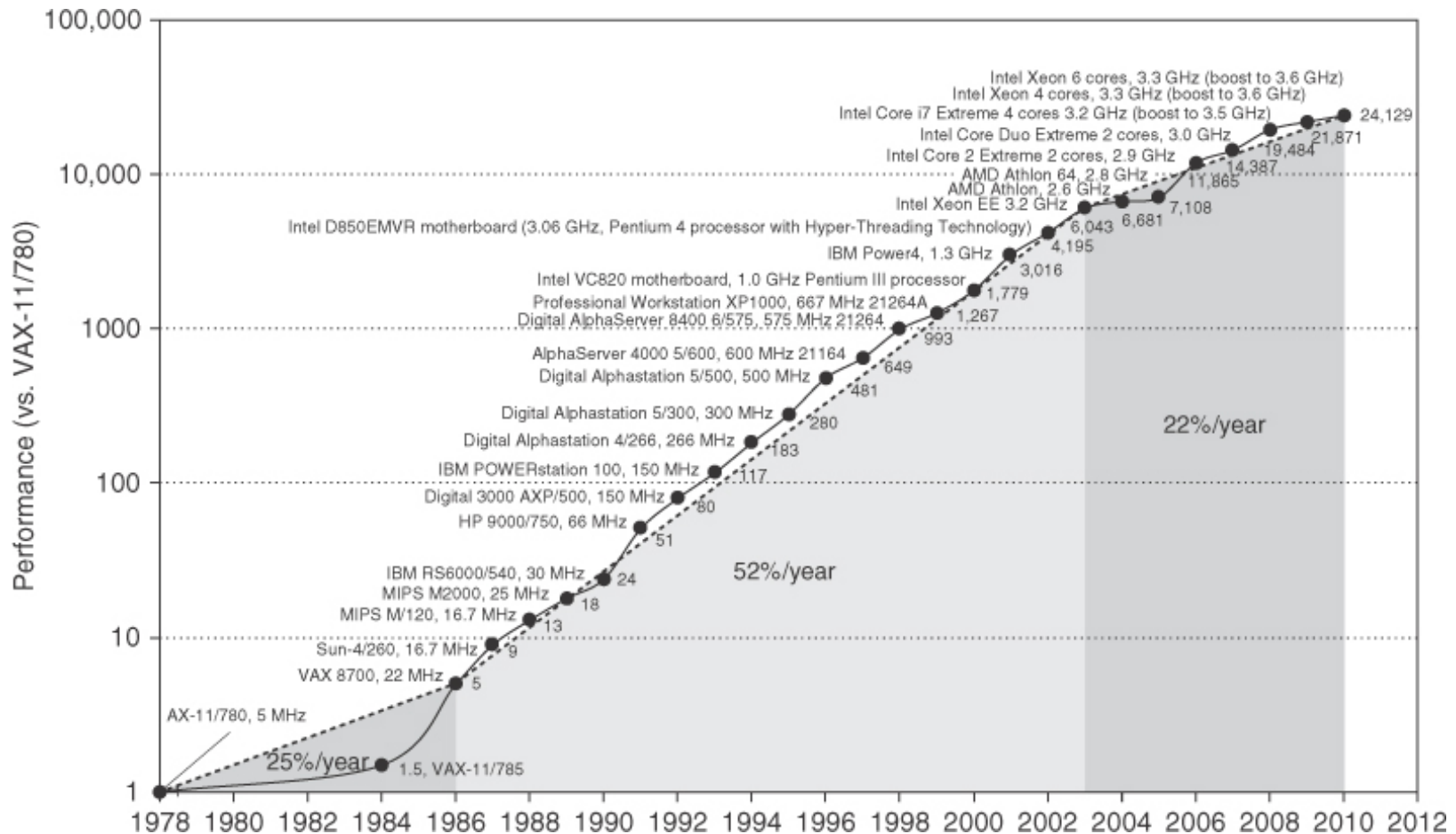
- ▣ How to fix?



Estimated Class Schedule

- Moore's Law, power wall, bandwidth wall
- Use of abstractions
- Assembly language
- Computer arithmetic
- Pipelining
- Using predictions
- Memory hierarchies
- Reliability and Security

Growth in Processor Performance

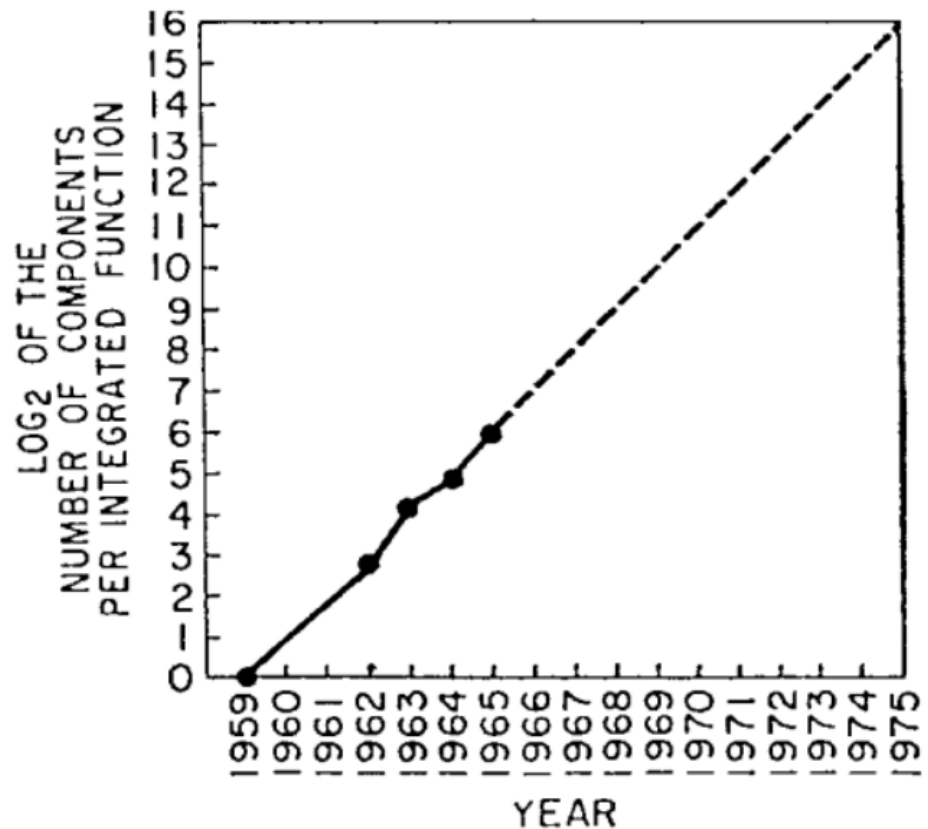


Growth in Processor Performance

- Main sources of the performance improvement
 - ▣ Enhanced underlying technology (semiconductor)
 - Faster and smaller transistors (Moore's Law)
 - ▣ Improvements in computer organization/architecture
 - How to better utilize the additional resources to gain more power savings, functionalities, and processing speed.

Moore's Law

- Moore's Law (1965)
 - ▣ Transistor count doubles every year
- Moore's Law (1975)
 - ▣ Transistor count doubles every two years



Source: G.E. Moore, "Cramming more components onto integrated circuits," 1965

What are New Challenges?

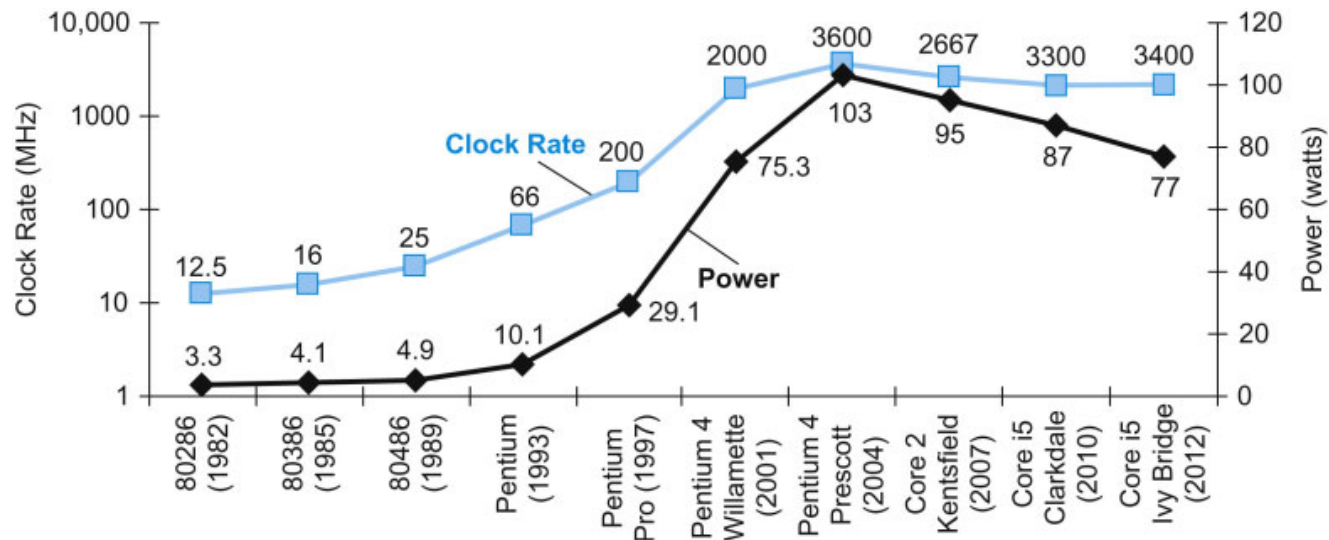
- Resources (transistors) on a processor chip?
- Can we use all of the transistors?
- Who is affected?
 - ▣ .

What are New Challenges?

- Resources (transistors) on a processor chip?
 - ▣ Not really, billions of transistors on a single chip.
- Can we use all of the transistors?
 - ▣ Due to **energy-efficiency** limitations, only a fraction of the transistor can be turned on at the same time!
- Who is affected?
 - ▣ Server computers by the peak power
 - ▣ Mobile and wearables due to energy-efficiency

Power Consumption Trends

- $\text{Power} = P_{\text{dynamic}} + P_{\text{static}}$
- $P_{\text{dynamic}} = \alpha \times C \times V^2 \times f$
- $P_{\text{static}} = V \times I_{\text{static}}$



Source: Hennessy & Patterson Textbook

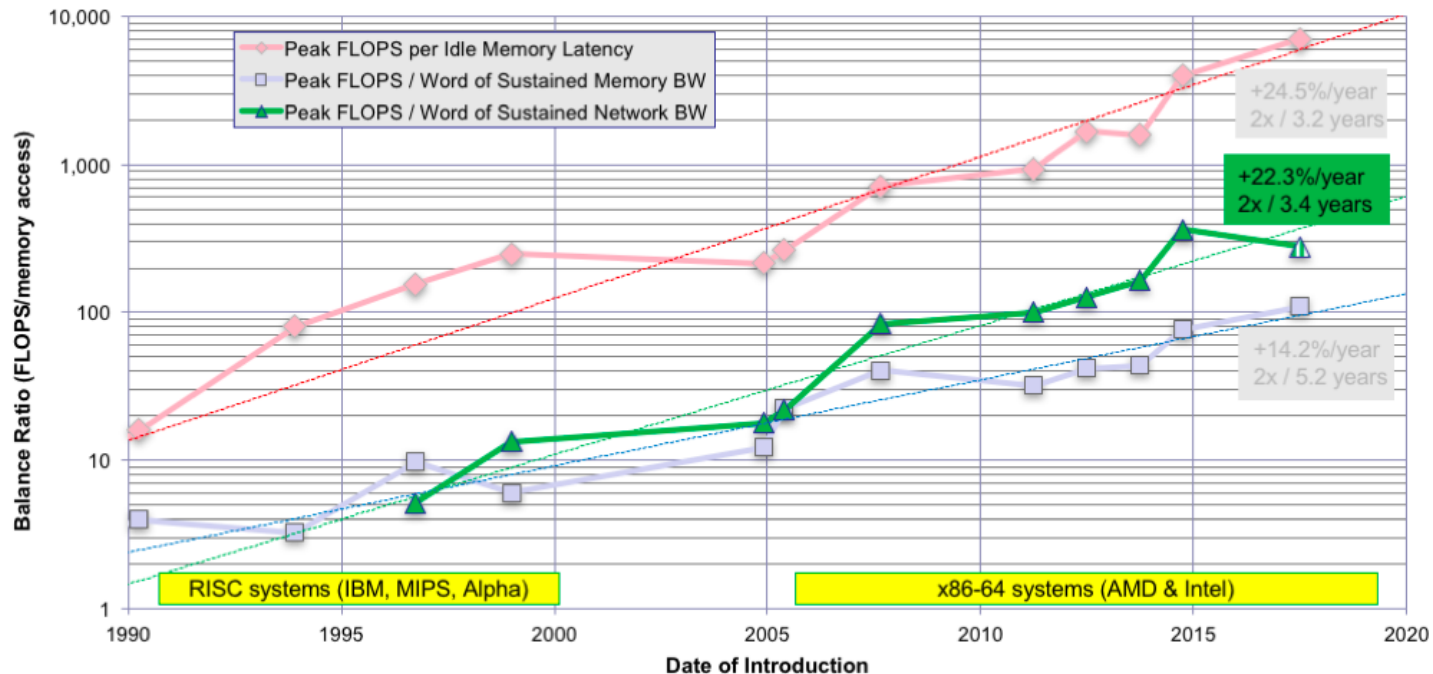
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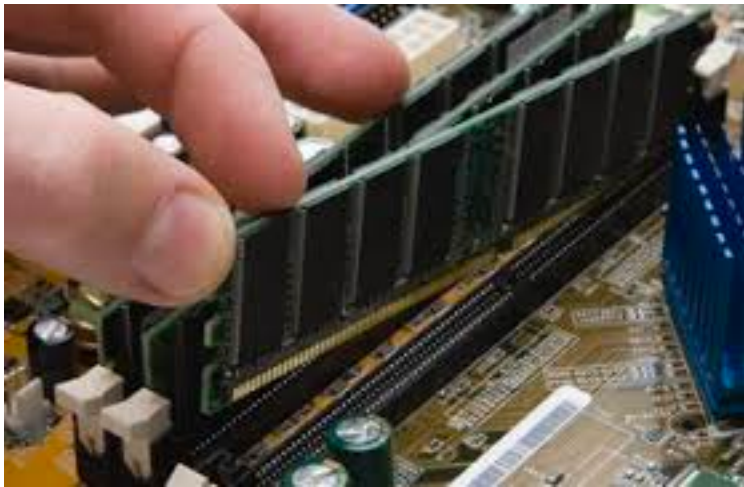
Interconnect Bandwidth is Falling Behind at a comparable rate



What are New Challenges?

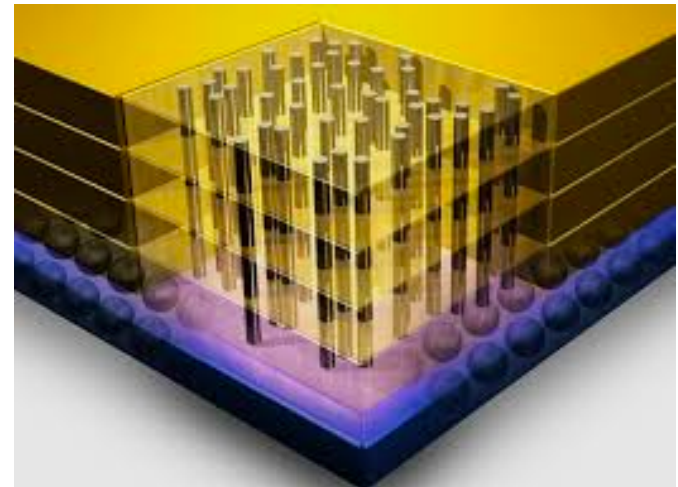
- Can in-package memory solve the problem?

Off-chip Memory



Lower Bandwidth
Lower Costs

3D Stacked Memory



Higher Bandwidth
Higher Costs

What are New Challenges?

- Protecting data against side channel attacks is a serious need
- Performance in the past 40 years increased
 - ▣ hardware speculation to exploit more **instruction level parallelism**
 - ▣ shared memories to facilitate **thread-level parallelism**
- What about security?
 - ▣ <https://meltdownattack.com/>



Unconventional Computing Systems

- How to program a Quantum computer?
 - ▣ Qbit vs. bit

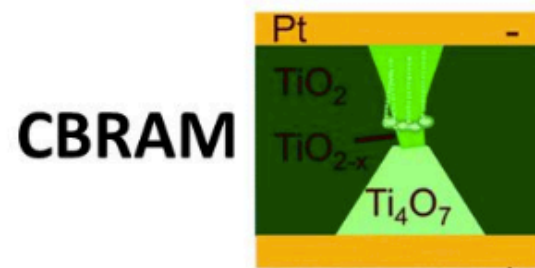
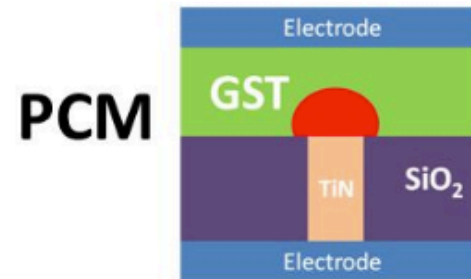
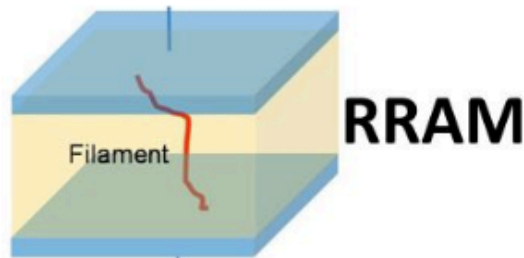
The screenshot displays the IBM Quantum Computing interface. At the top, there is a navigation bar with "Quantum Experience", "Account", and "Logout". Below this, a "Directions" panel shows a qubit connectivity diagram, and a "Qubit 0 properties" panel lists: $f = 5.35 \text{ GHz}$, $T_1 = 54 \mu\text{s}$, $T_2 = 74.3 \mu\text{s}$, $\epsilon_2 = 2.6 \times 10^{-3}$, and a timestamp "2016-04-27 02:47".

The main workspace is titled "Composer" and shows a quantum circuit named "Grover's Search Algorithm, 11" on a "Real Quantum Processor". The circuit involves five qubits, Q_0 through Q_4 , all initialized to $|0\rangle$. The circuit consists of several layers of gates: H gates on Q_1 and Q_2 ; H gates on Q_1 and Q_2 followed by a CNOT gate with Q_1 as control and Q_2 as target; H gates on Q_1 and Q_2 followed by X gates on Q_1 and Q_2 ; H gates on Q_1 and Q_2 followed by another CNOT gate with Q_1 as control and Q_2 as target; H gates on Q_1 and Q_2 followed by X gates on Q_1 and Q_2 ; and finally H gates on Q_1 and Q_2 . The circuit concludes with measurement operations on Q_1 and Q_2 .

At the bottom, a "GATES" toolbar includes buttons for Id , X , Z , Y , H , S , S^\dagger , a CNOT gate, T , T^\dagger , and "MEASURE". A "Simulate" button is also visible on the right side of the interface.

Emerging Non-volatile Memories

- Use resistive states to represent info.
 - ▣ Can we build non-von Neumann machines?
 - In-Memory and In-situ computers



Next Class

- Lecture: Measuring Performance
- Todo: order the textbook